



Digital Integrated Circuits

A Design Perspective

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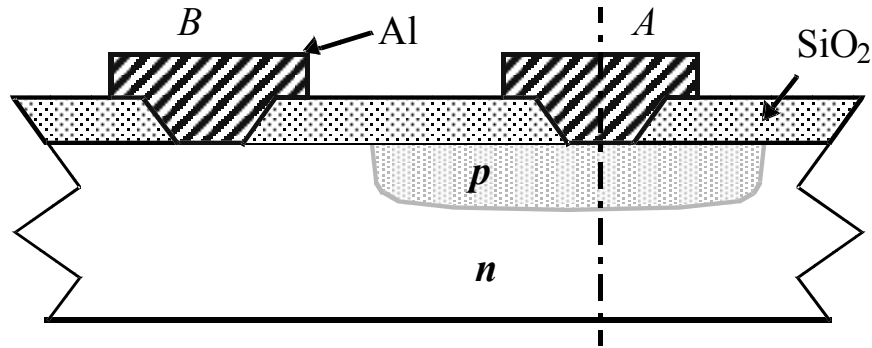
The Devices

July 30, 2002

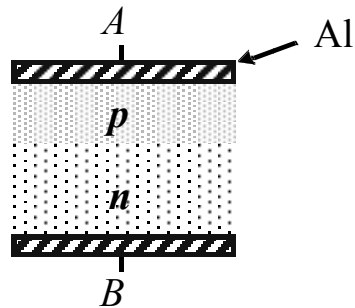
Goal of this chapter

- ❑ Present intuitive understanding of device operation**
- ❑ Introduction of basic device equations**
- ❑ Introduction of models for manual analysis**
- ❑ Introduction of models for SPICE simulation**
- ❑ Analysis of secondary and deep-sub-micron effects**
- ❑ Future trends**

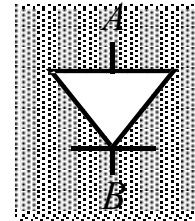
The Diode



Cross-section of *pn*-junction in an IC process



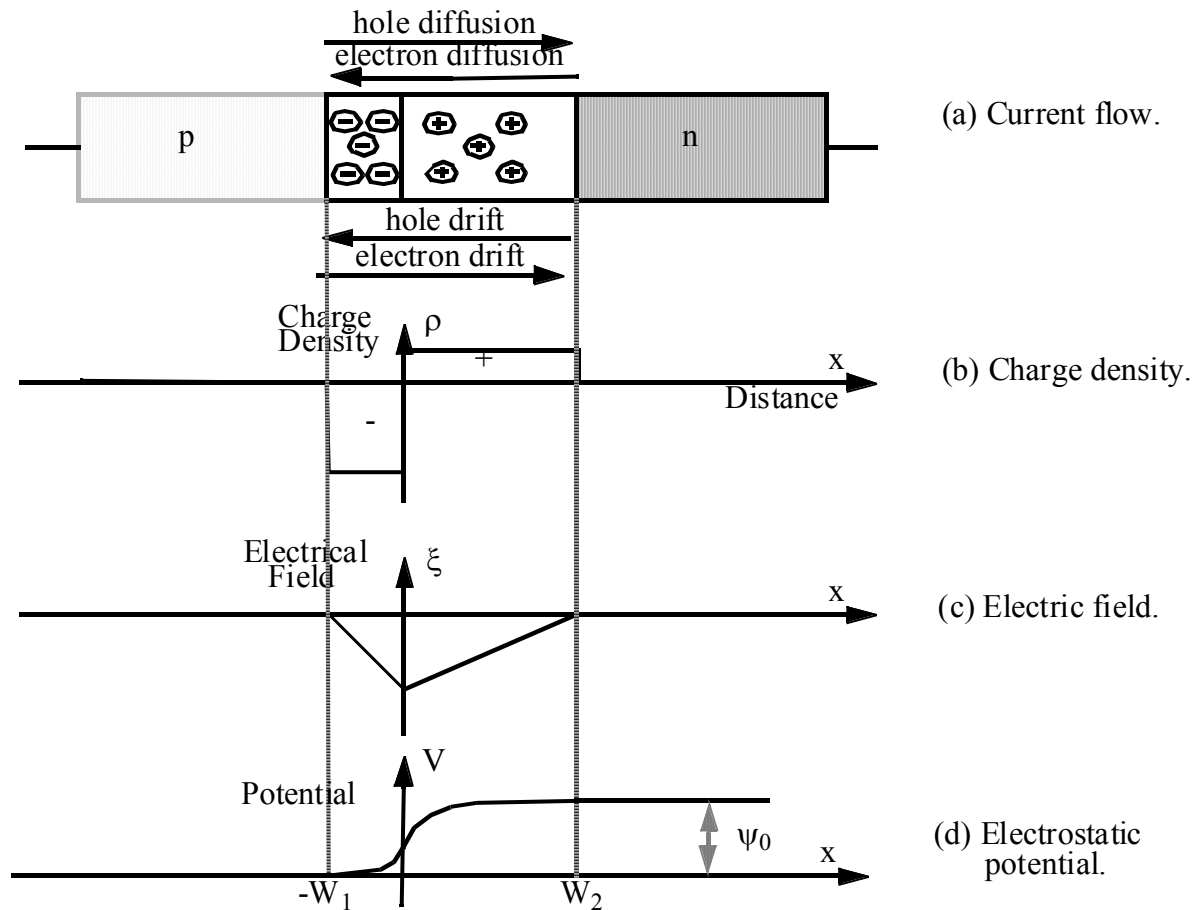
One-dimensional representation



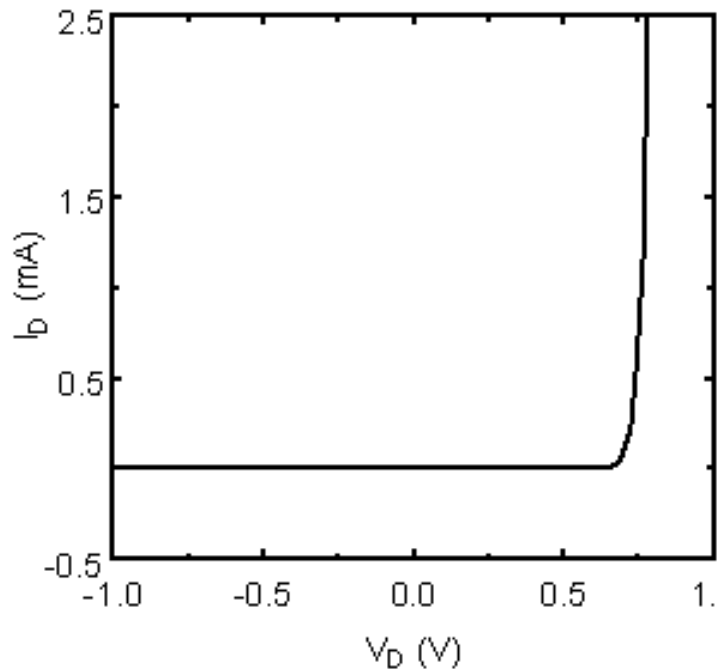
diode symbol

Mostly occurring as parasitic element in Digital ICs

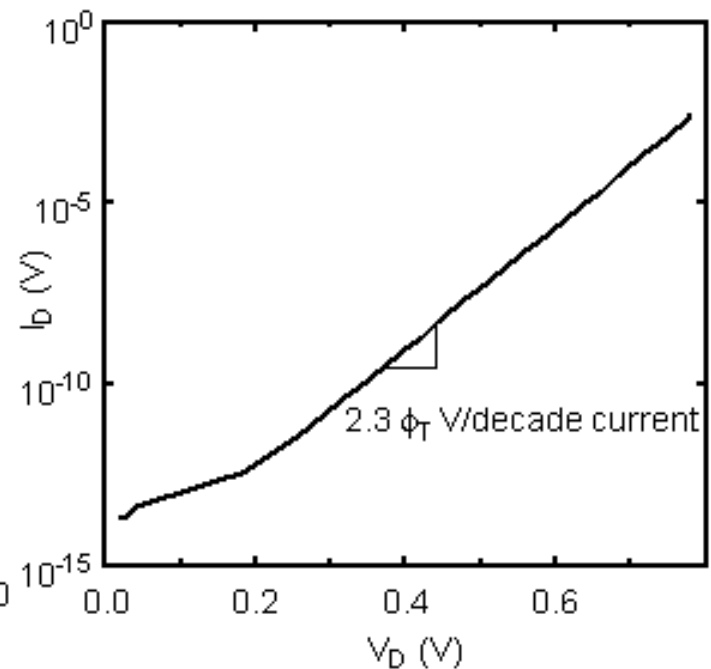
Depletion Region



Diode Current



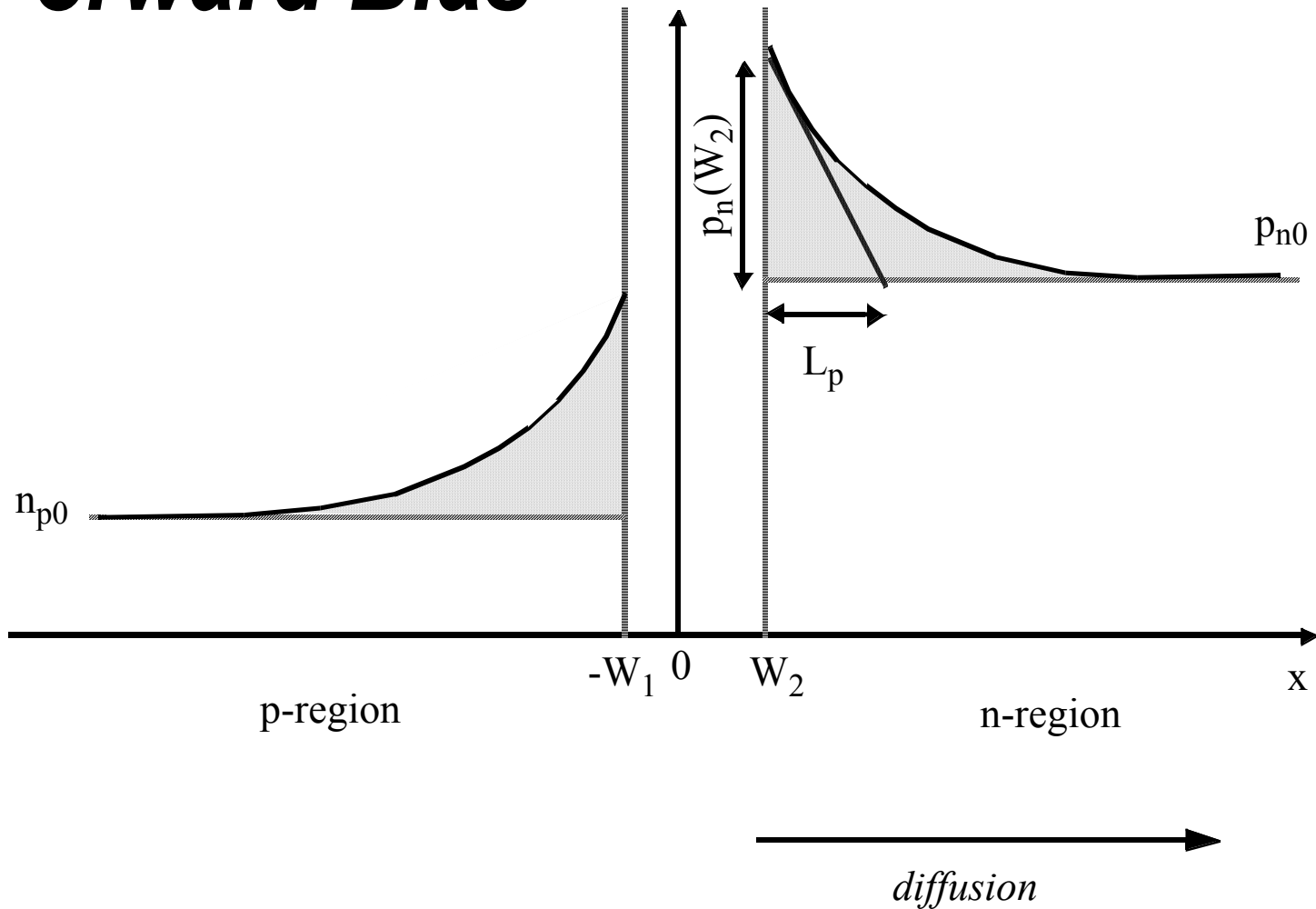
(a) On a linear scale.



(b) On a logarithmic scale (forward bias).

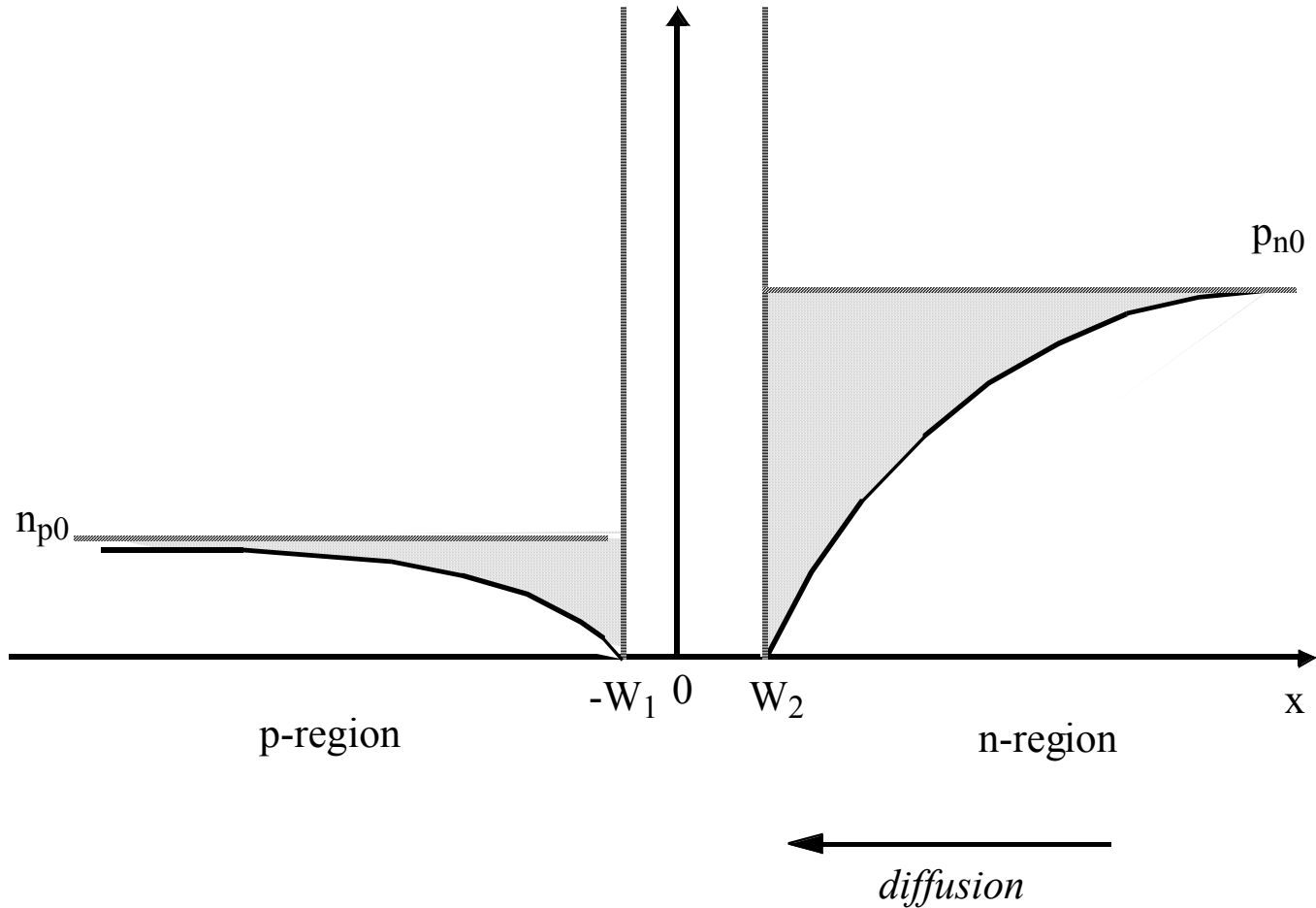
$$I_D = I_S \left(e^{V_D / \phi_T} - 1 \right)$$

Forward Bias



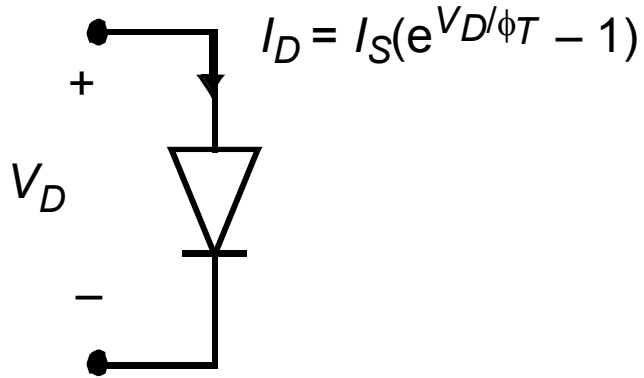
Typically avoided in Digital ICs

Reverse Bias

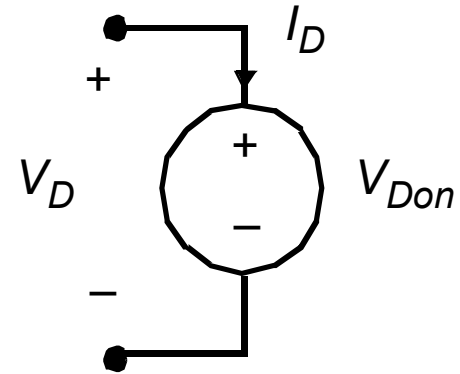


The Dominant Operation Mode

Models for Manual Analysis

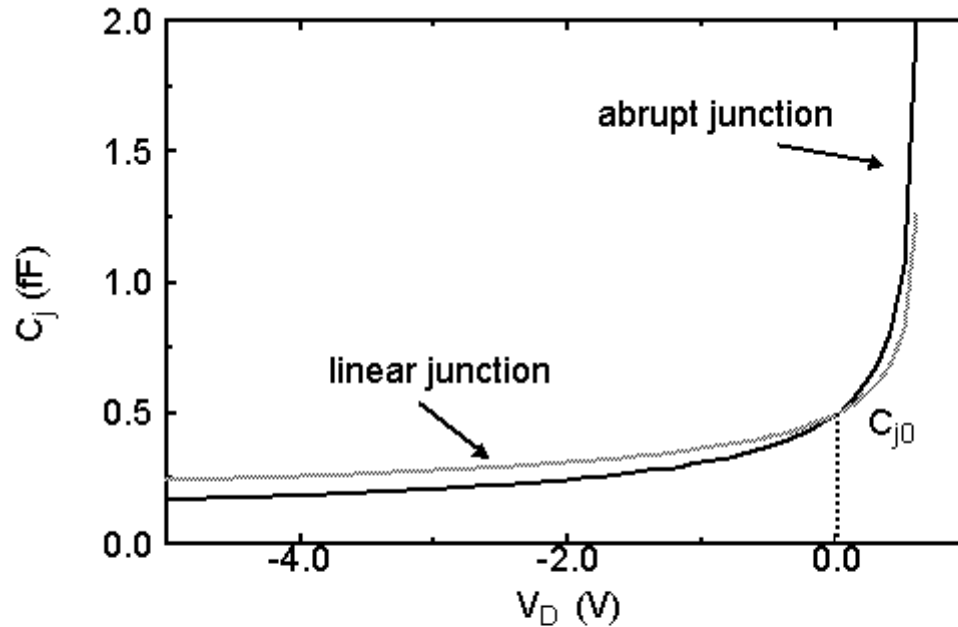


(a) Ideal diode model



(b) First-order diode model

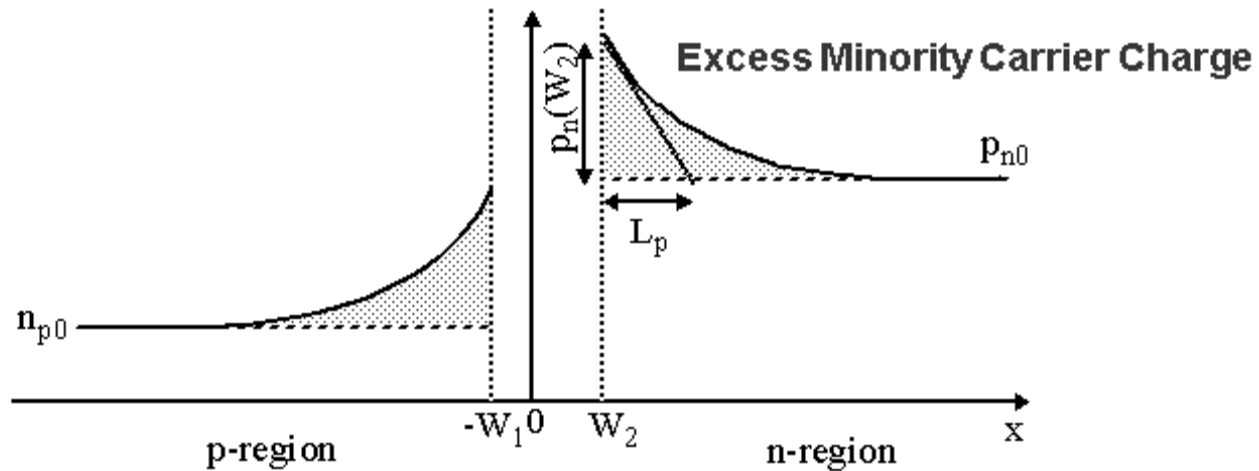
Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

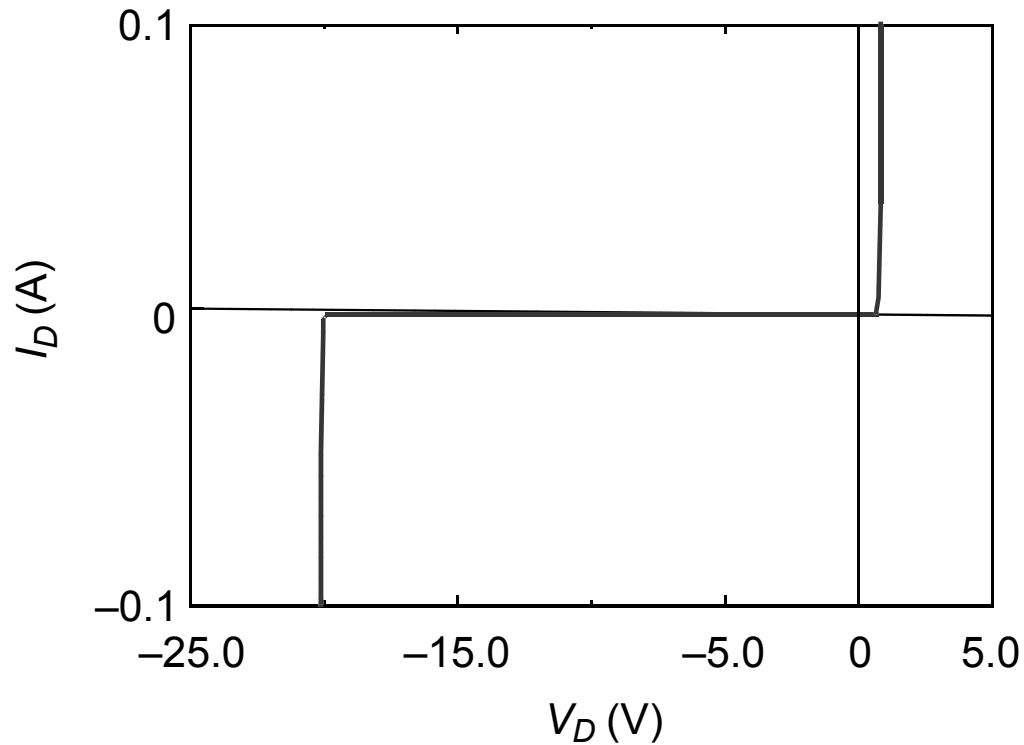
$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction

Diffusion Capacitance



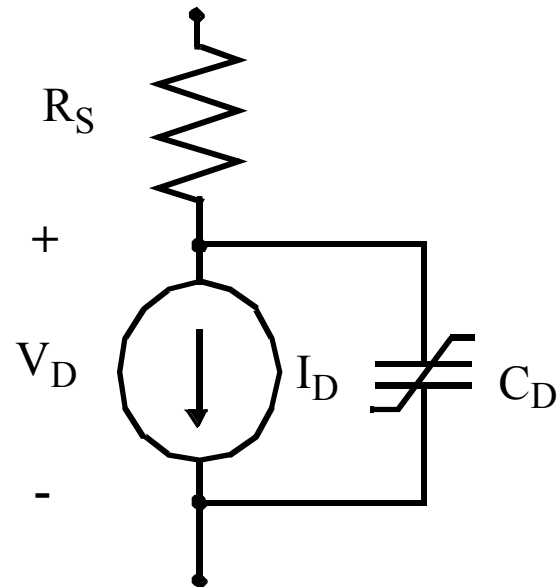
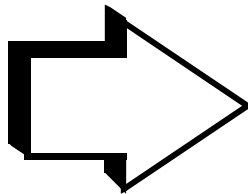
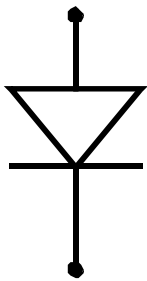
$$C_d = \frac{dQ_D}{dV_D} = \tau_T \frac{dI_D}{dV_D} \approx \frac{\tau_T I_D}{\phi_T}$$

Secondary Effects



Avalanche Breakdown

Diode Model



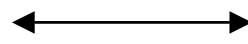
SPICE Parameters

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

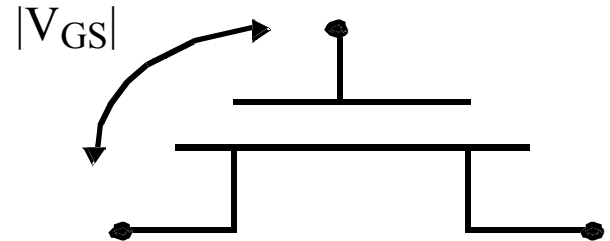
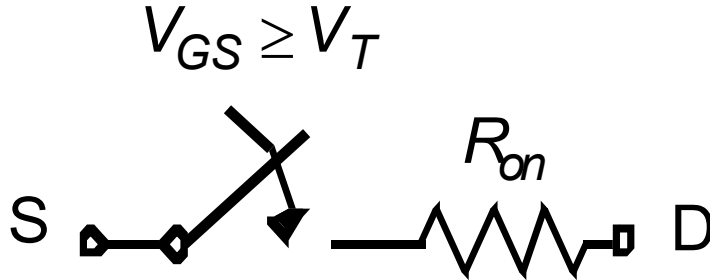
First Order SPICE diode model parameters.

What is a Transistor?

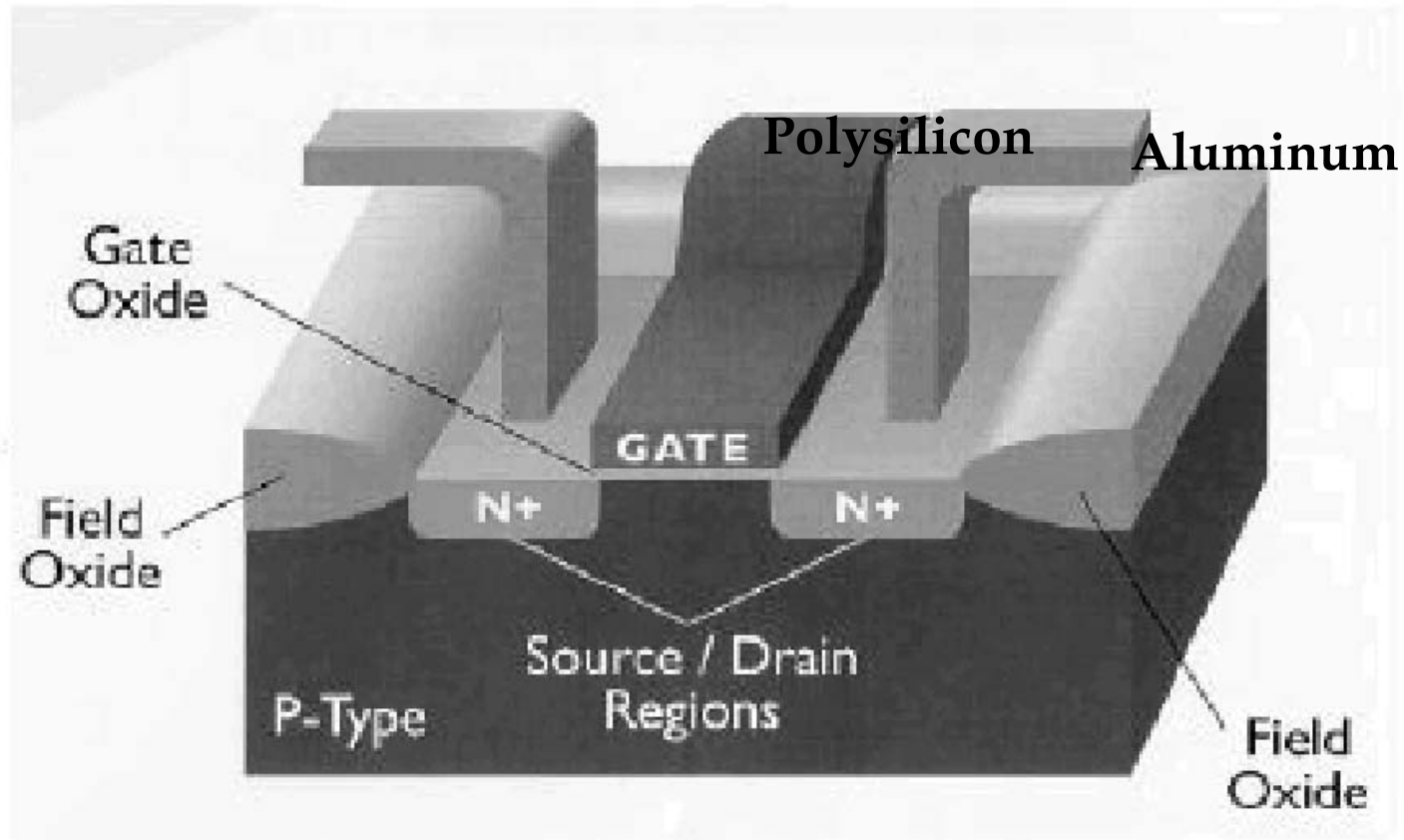
A Switch!



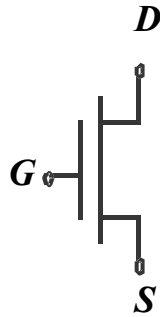
An MOS Transistor



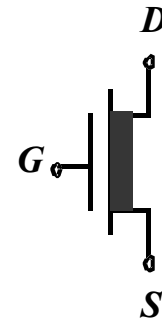
The MOS Transistor



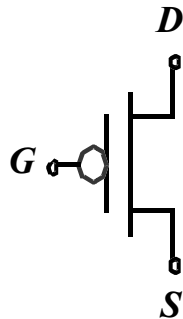
MOS Transistors - Types and Symbols



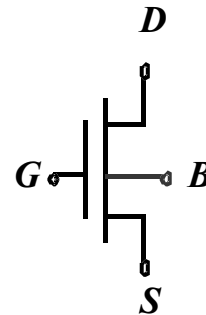
NMOS Enhancement



NMOS Depletion

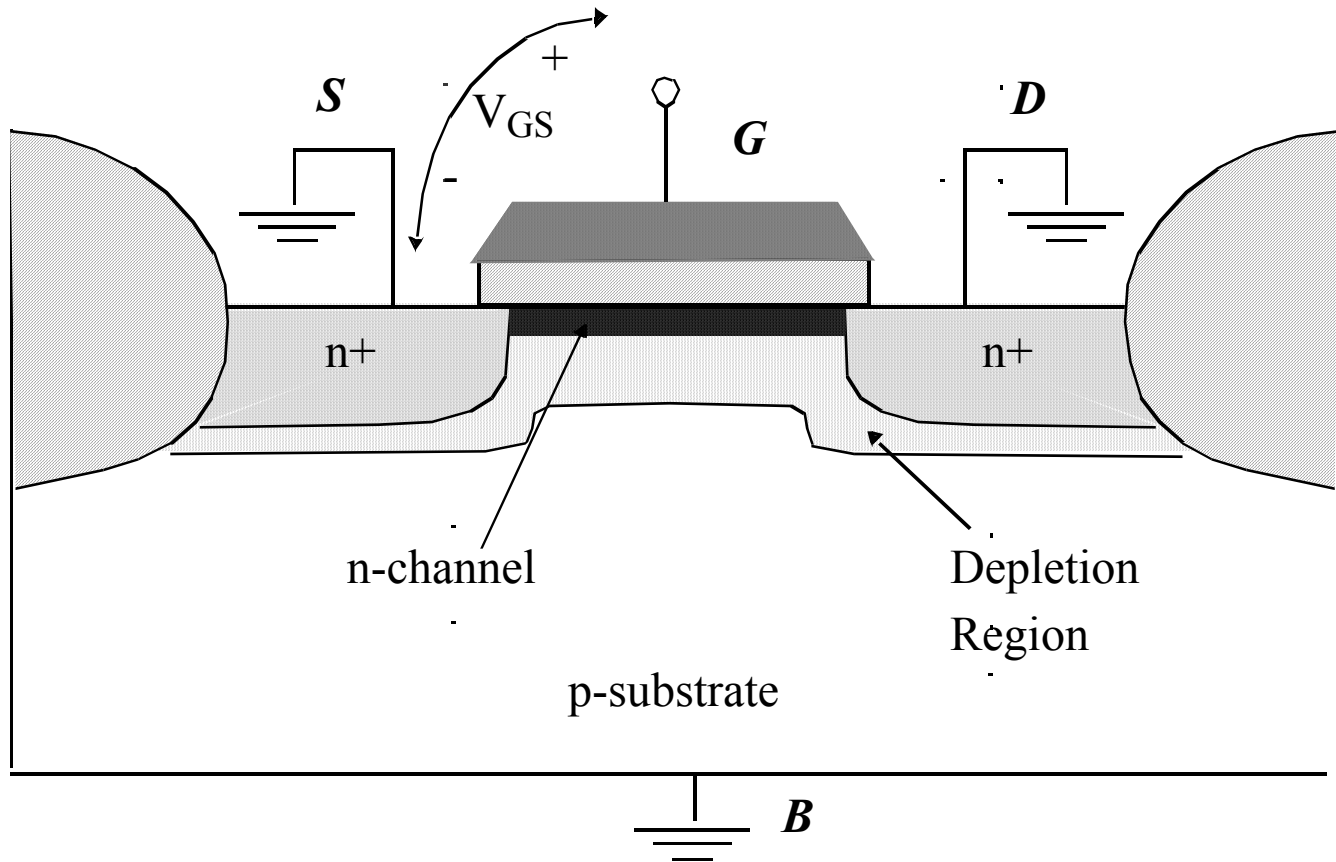


PMOS Enhancement



**NMOS with
Bulk Contact**

Threshold Voltage: Concept



The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference Depletion Layer Charge Surface Charge Implants

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Body Effect Coefficient

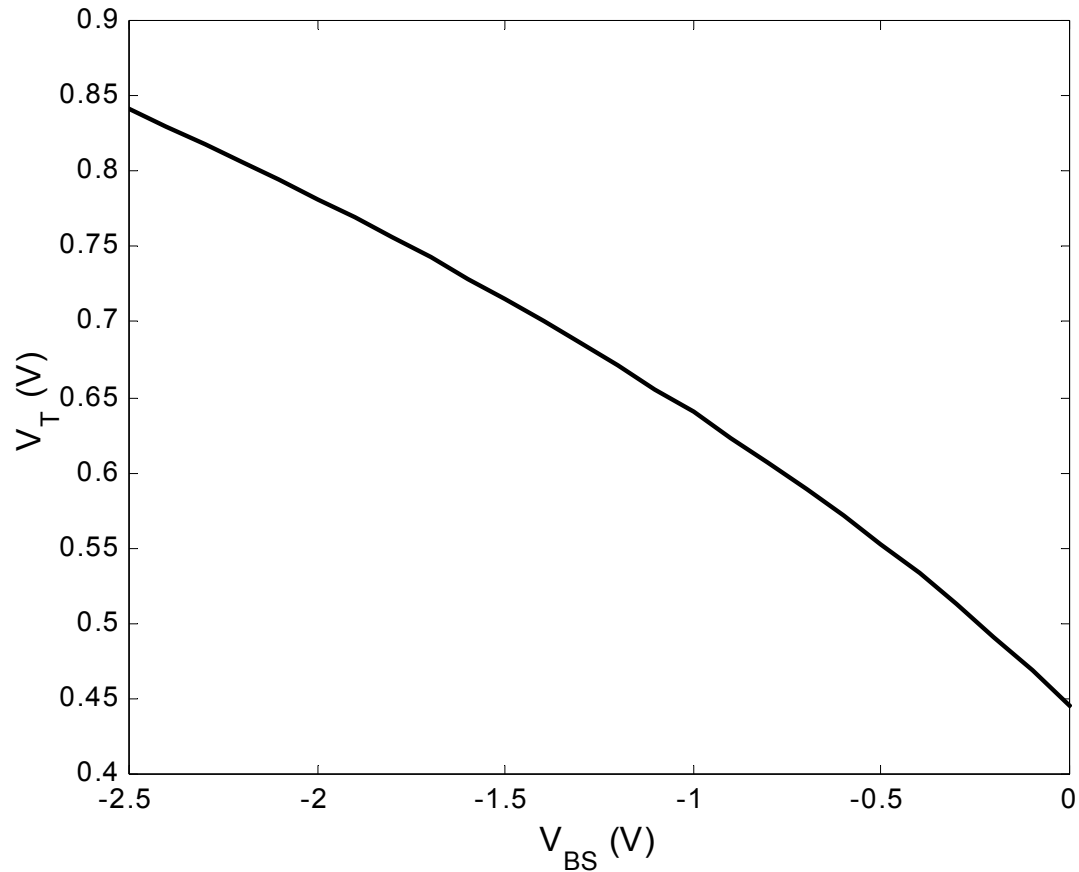
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

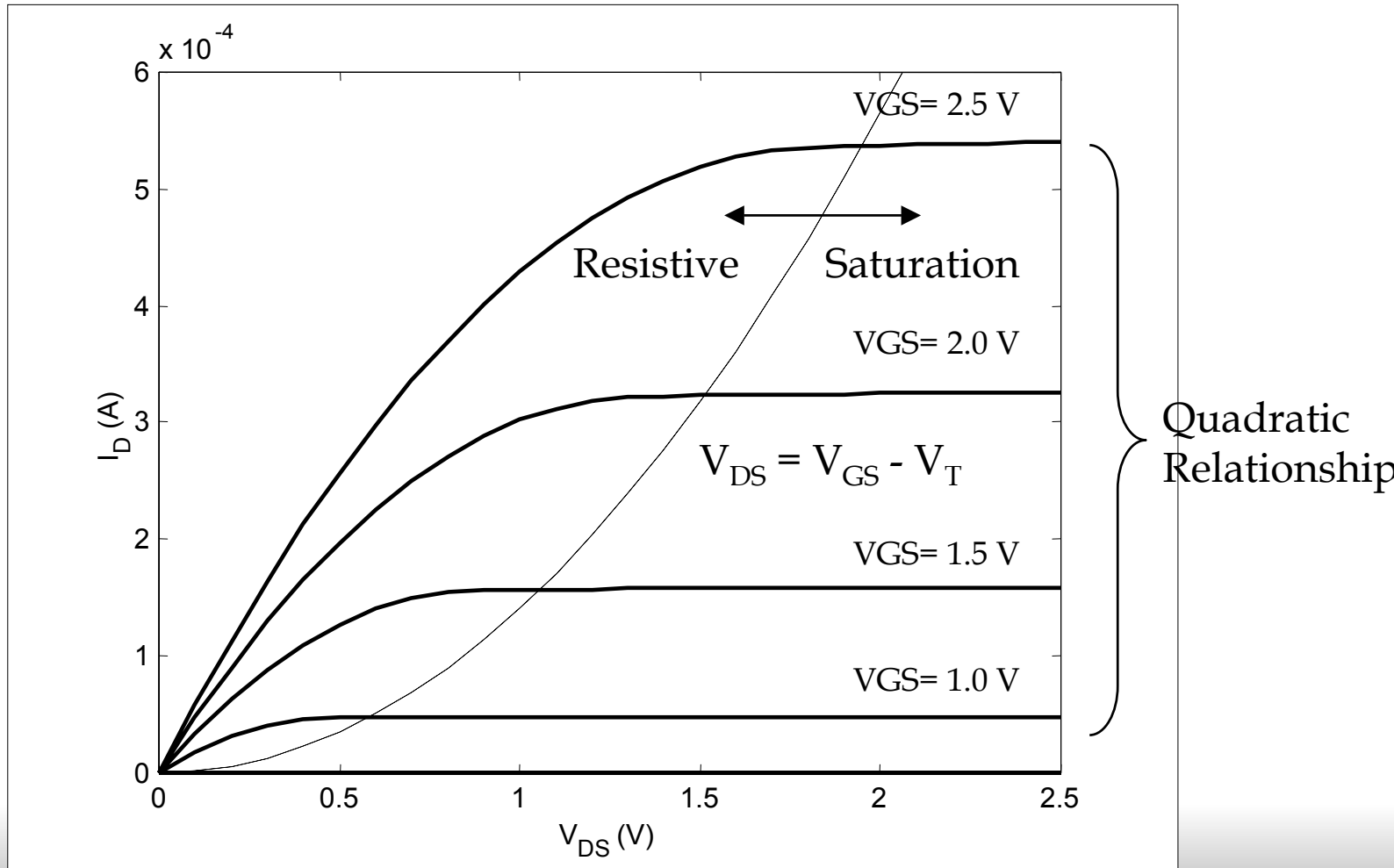
$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$

The Body Effect

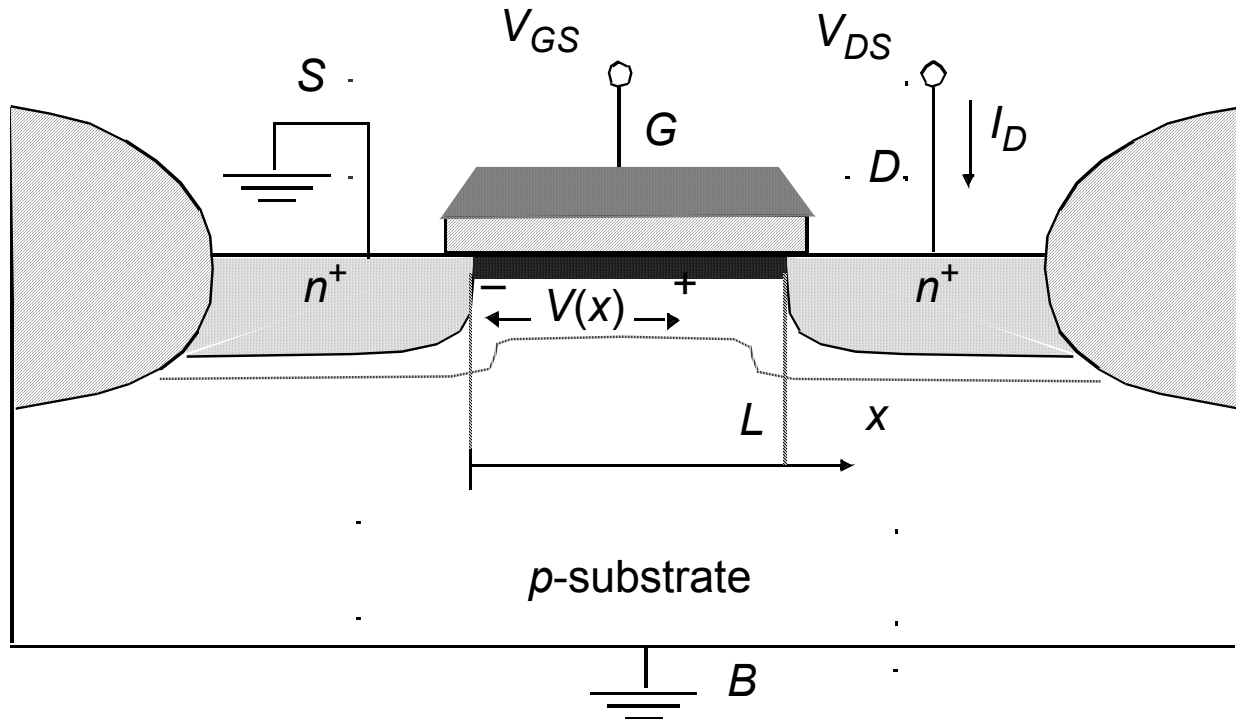


Current-Voltage Relations

A good ol' transistor

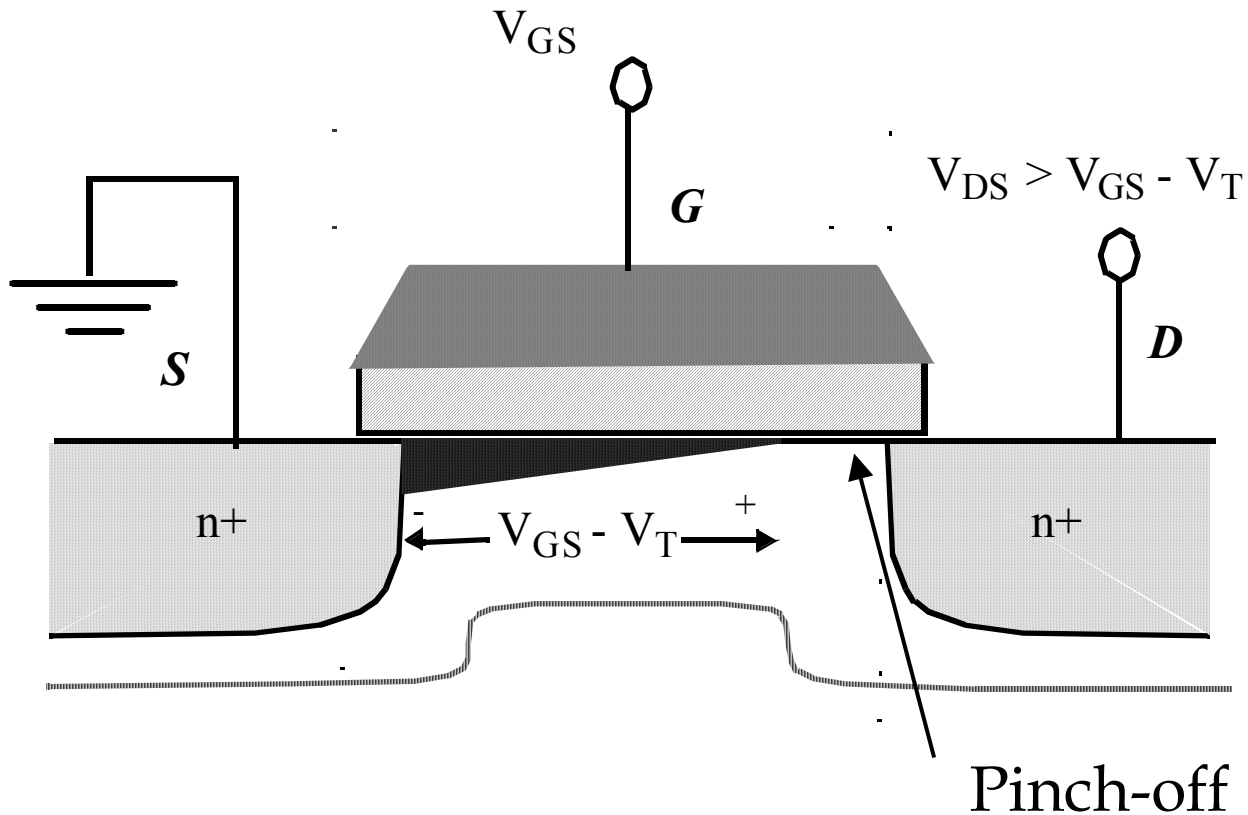


Transistor in Linear



MOS transistor and its bias conditions

Transistor in Saturation



Current-Voltage Relations

Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

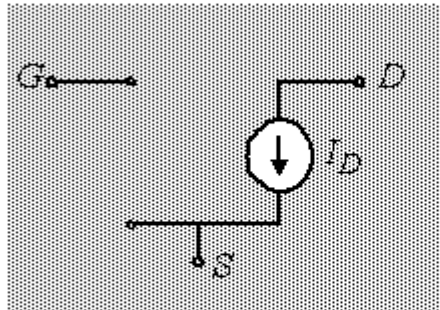
with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}} \quad \text{Process Transconductance Parameter}$$

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$ Channel Length Modulation

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

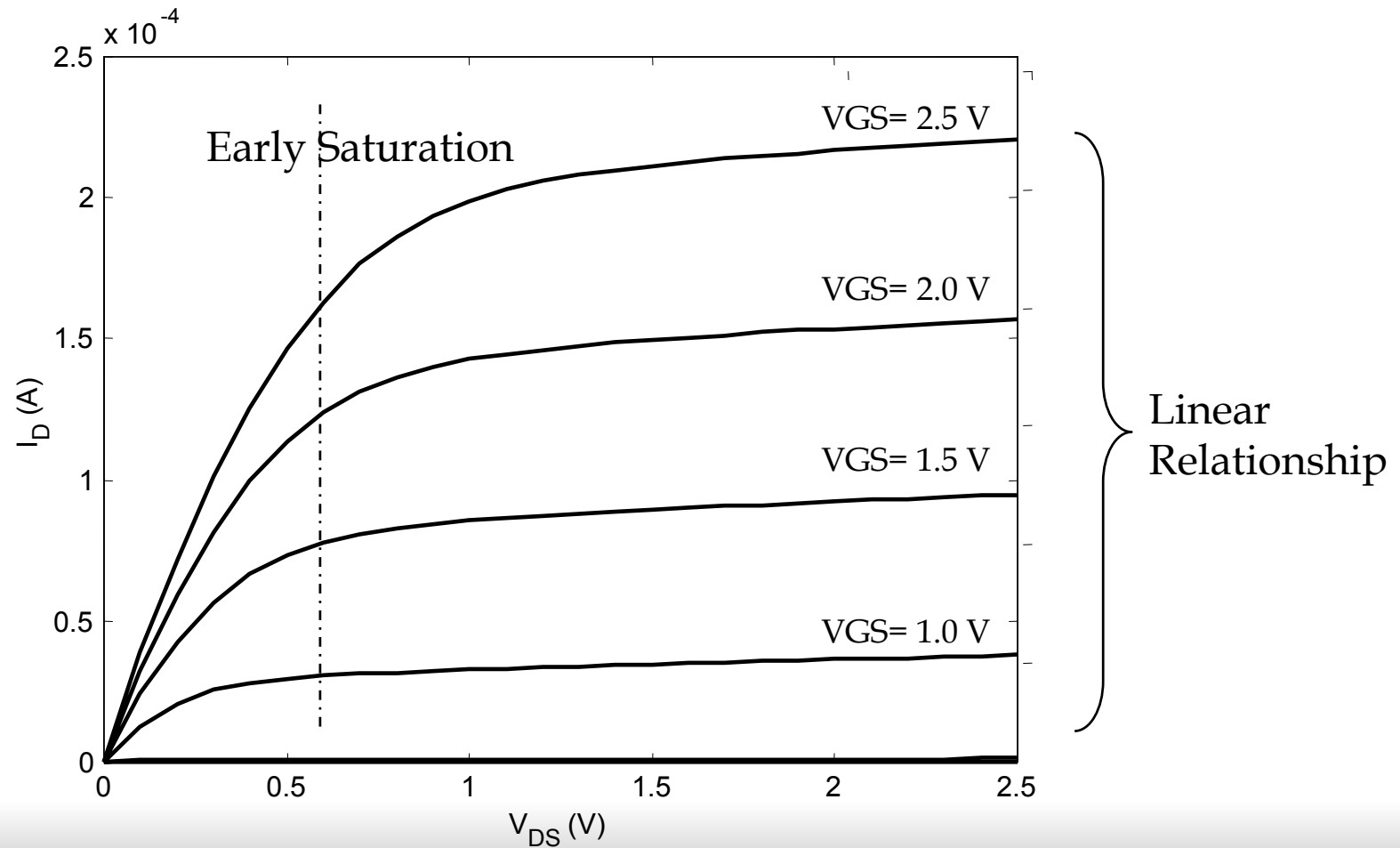
$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

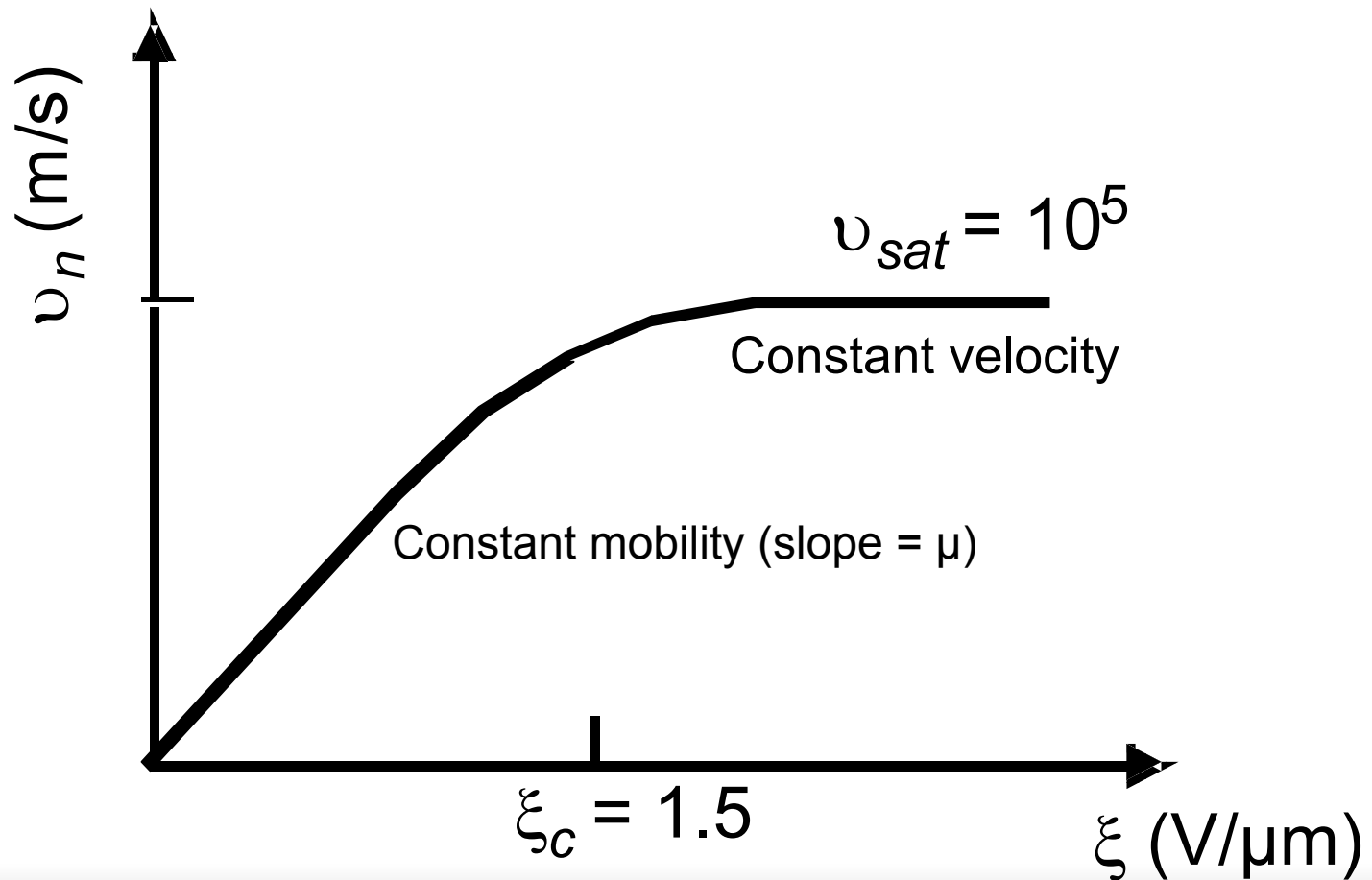
$$V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Current-Voltage Relations

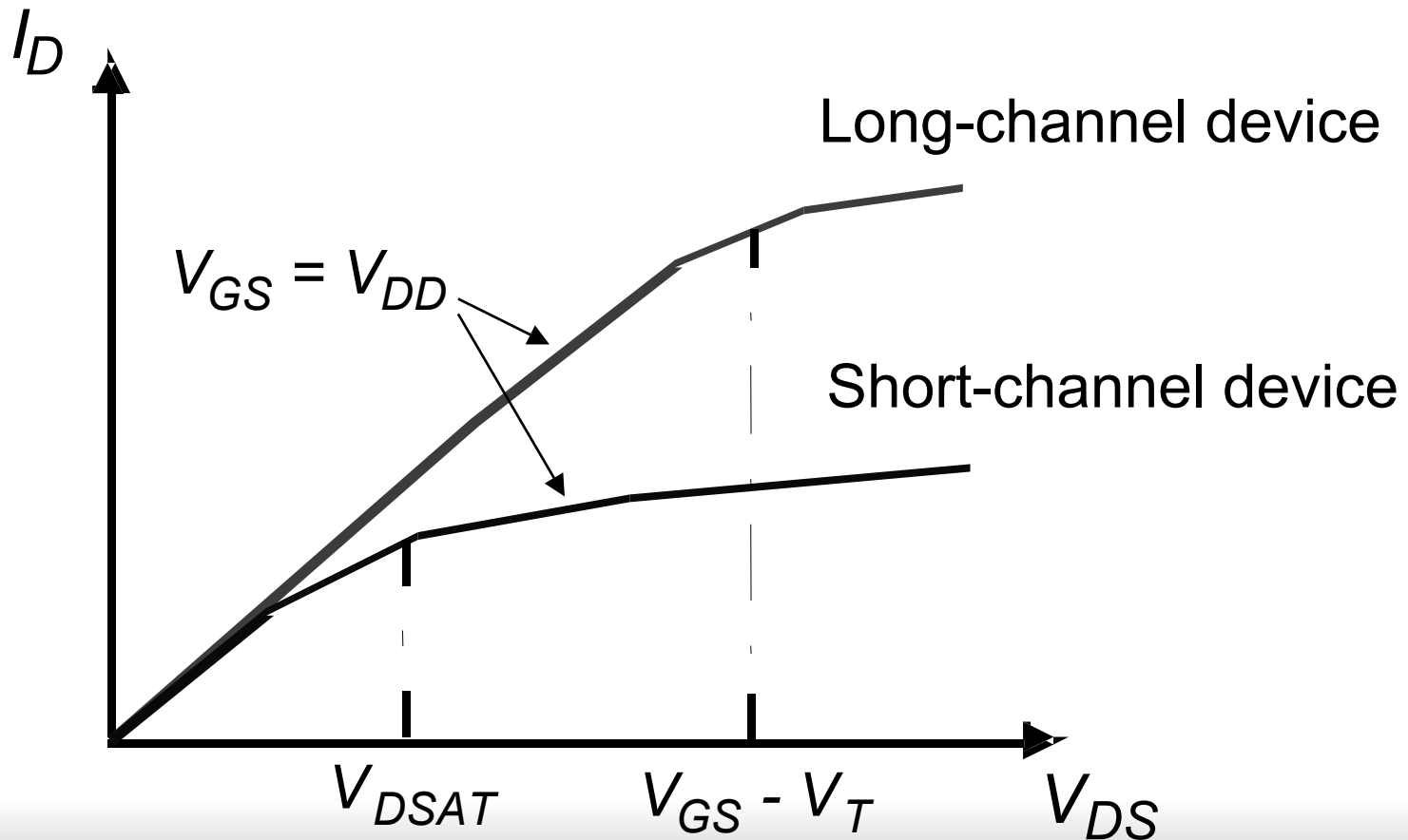
The Deep-Submicron Era



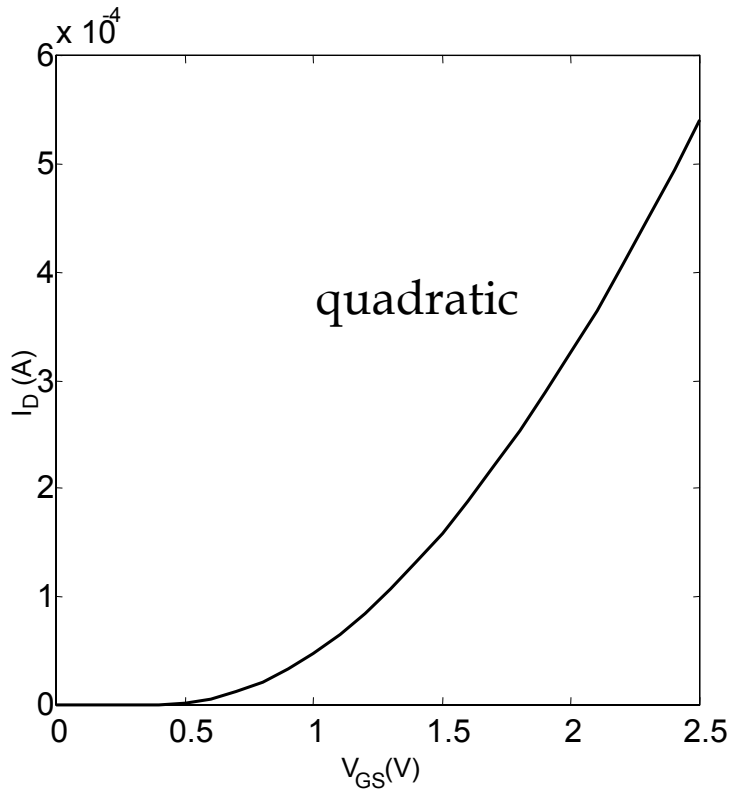
Velocity Saturation



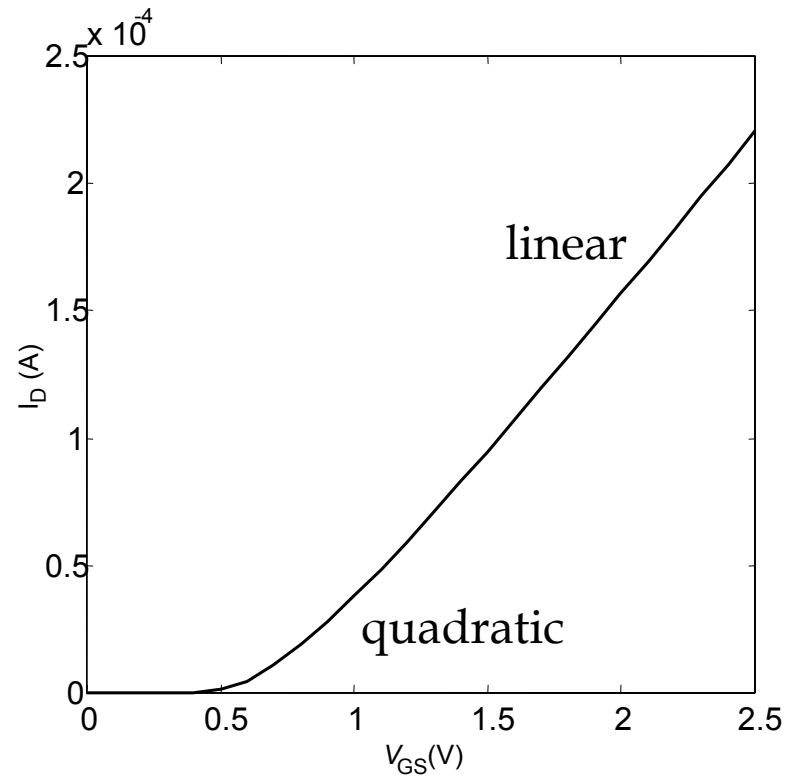
Perspective



I_D versus V_{GS}

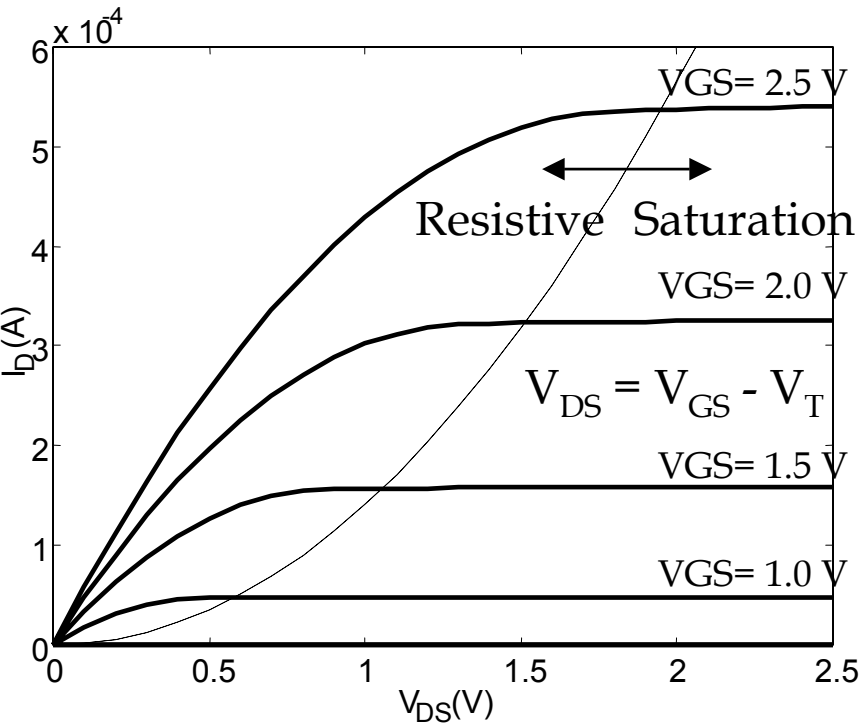


Long Channel

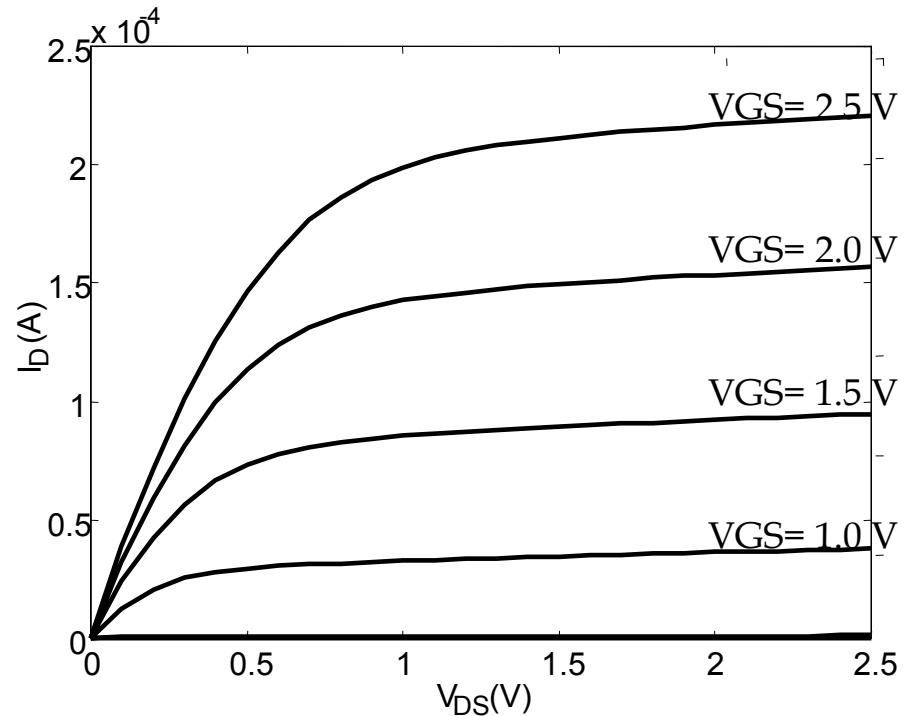


Short Channel

I_D versus V_{DS}

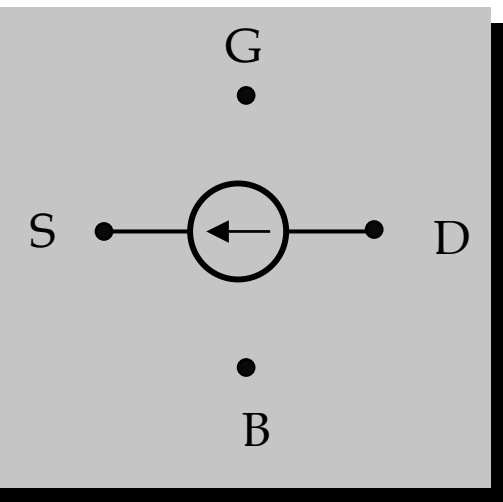


Long Channel



Short Channel

A unified model for manual analysis



$$I_D = 0 \quad \text{for } V_{GT} \leq 0$$

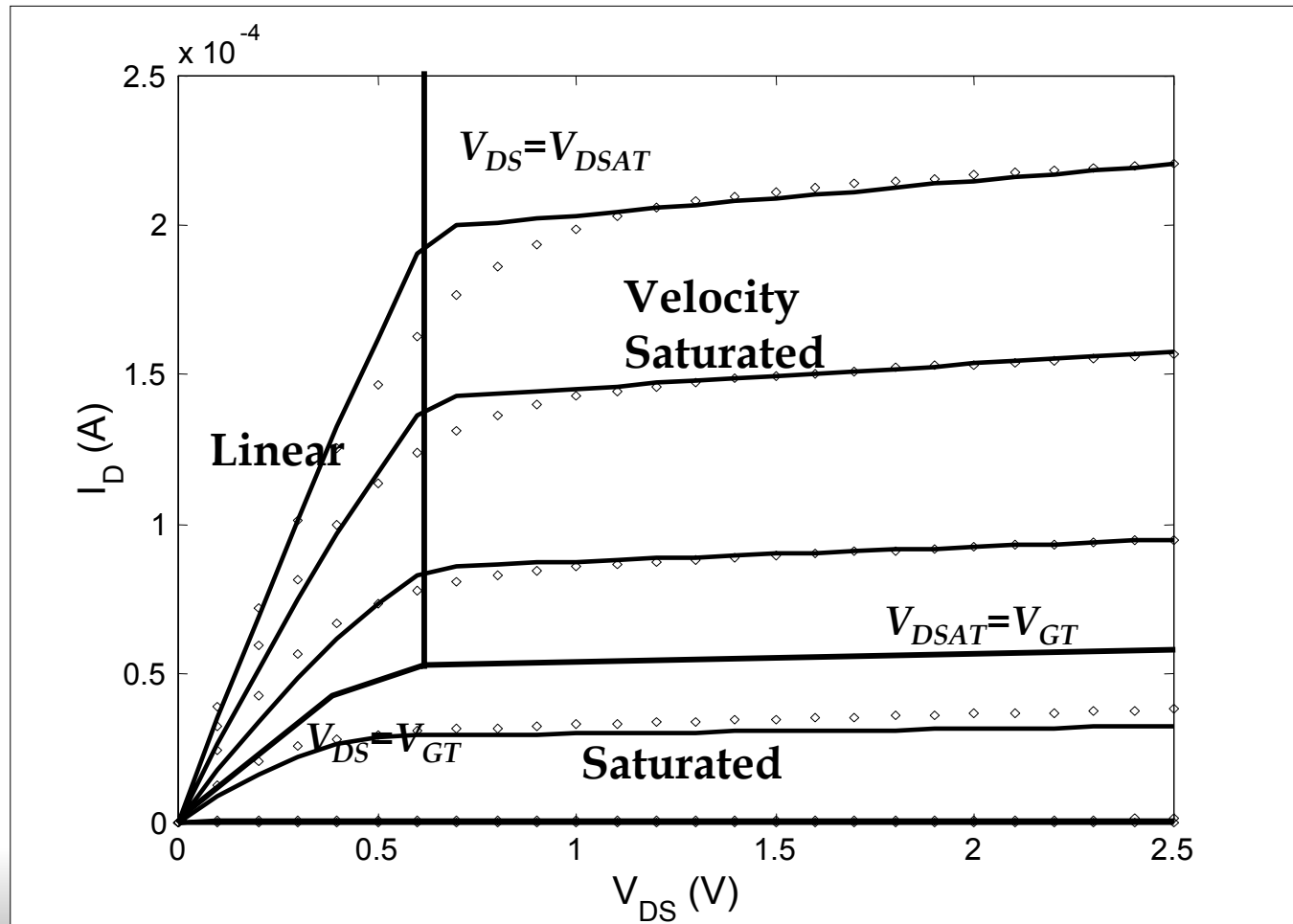
$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq$$

$$\text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

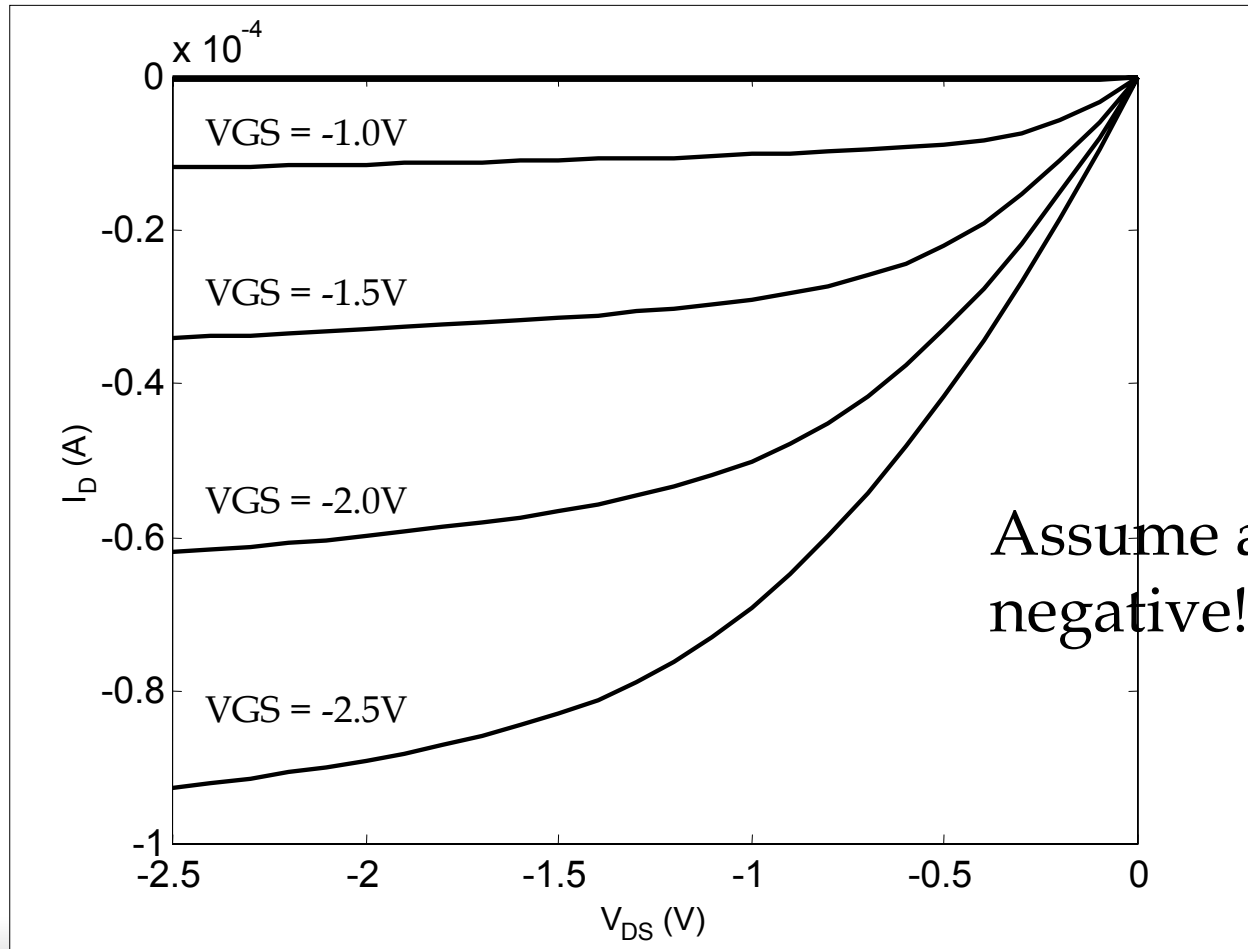
$$V_{GT} = V_{GS} - V_T,$$

$$\text{and } V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Simple Model versus SPICE



A PMOS Transistor



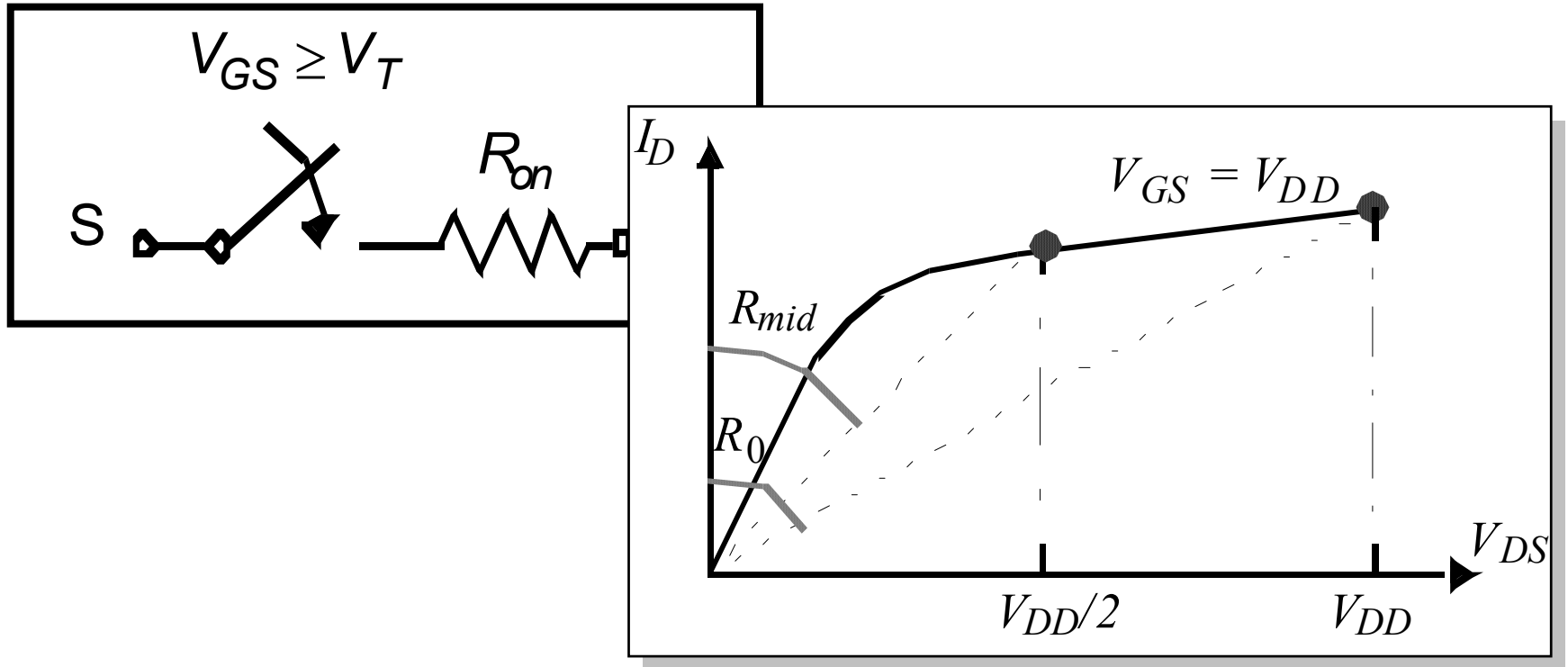
Assume all variables
negative!

Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

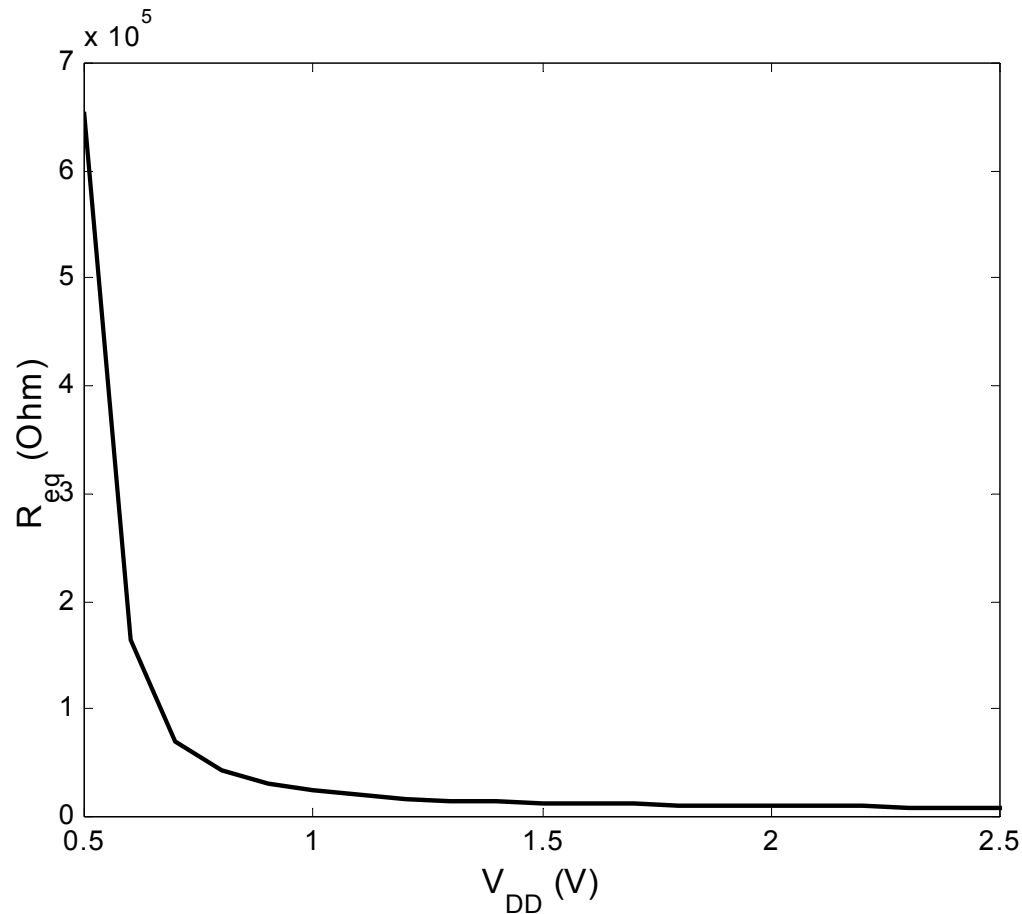
	V_{T0} (V)	γ ($\text{V}^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

The Transistor as a Switch



$$R_{eq} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

The Transistor as a Switch



The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} ($W/L = 1$) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L .

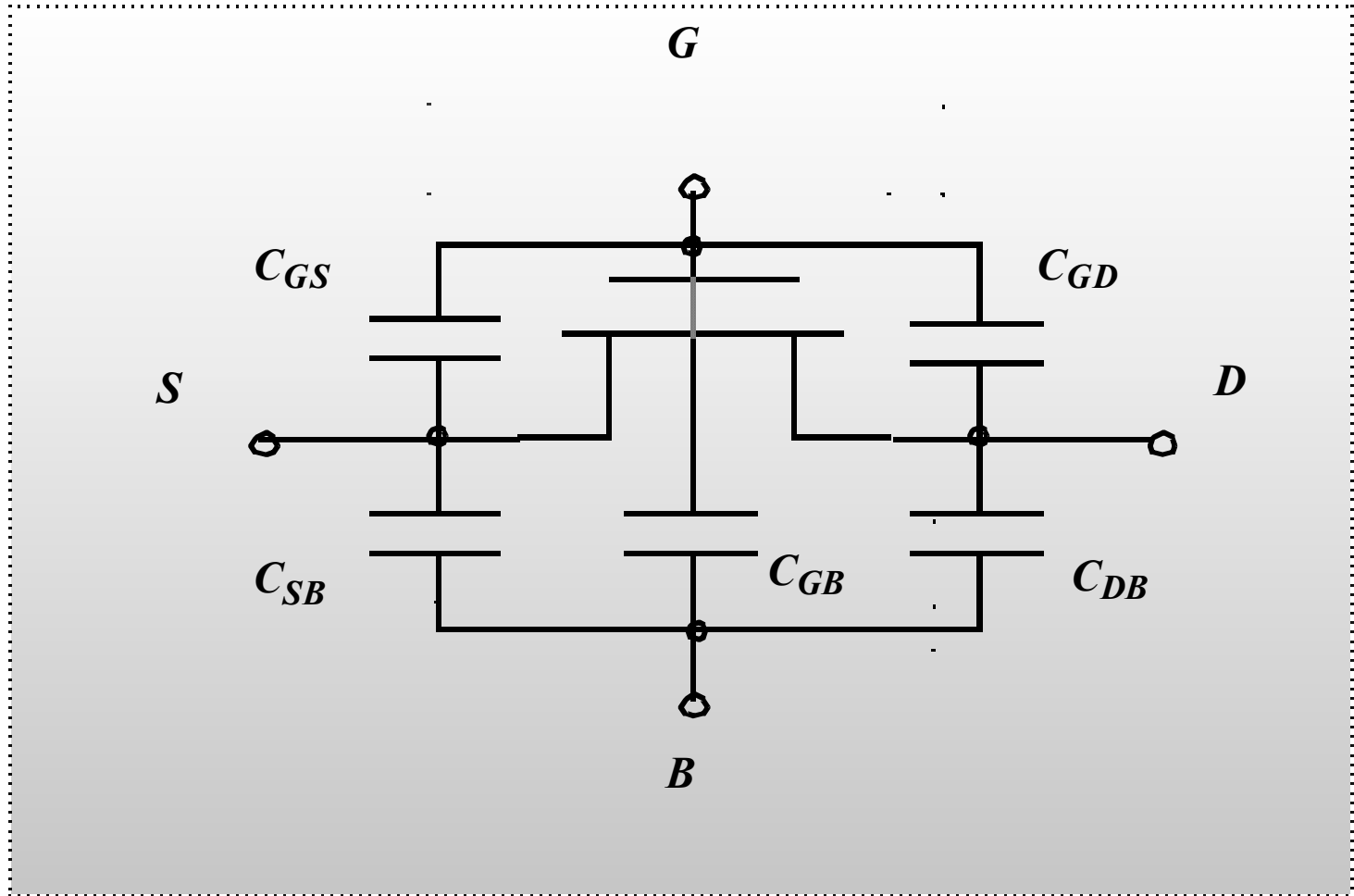
V_{DD} (V)	1	1.5	2	2.5
NMOS ($\text{k}\Omega$)	35	19	15	13
PMOS ($\text{k}\Omega$)	115	55	38	31

MOS Capacitances

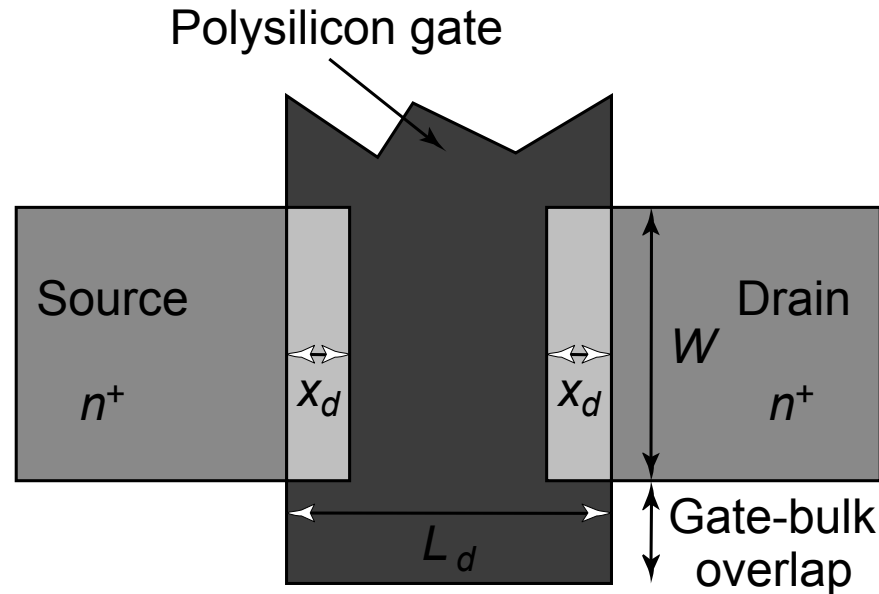
Dynamic Behavior



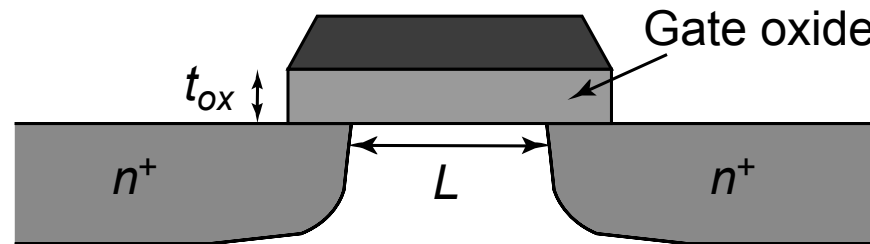
Dynamic Behavior of MOS Transistor



The Gate Capacitance



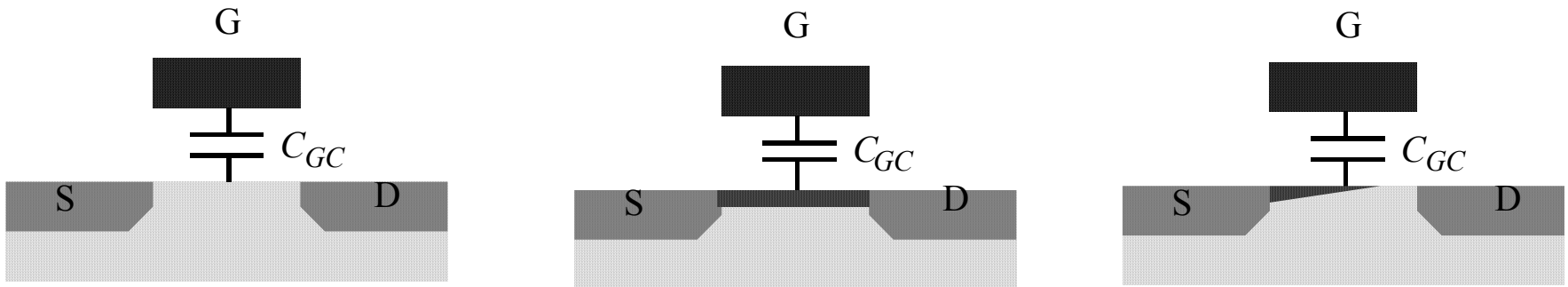
Top view



Cross section

$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$

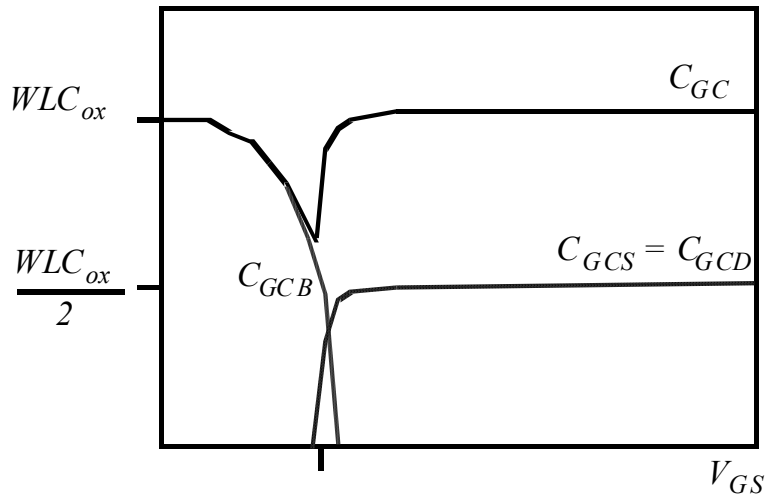
Gate Capacitance



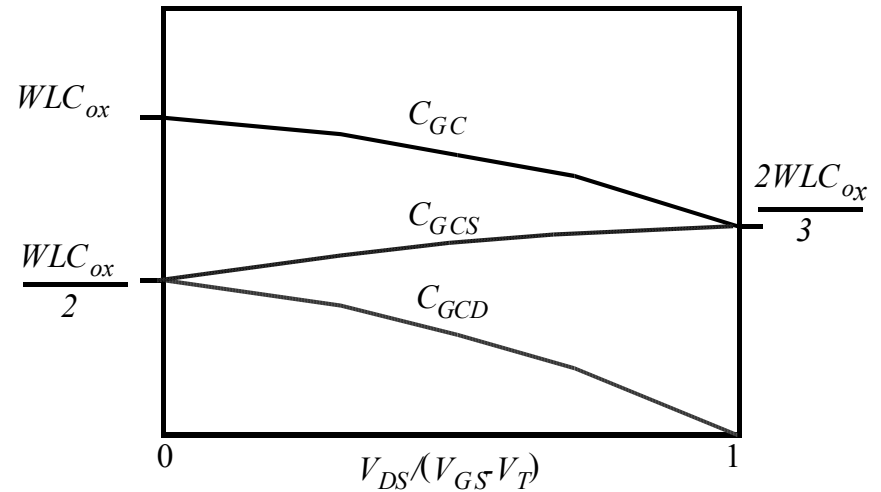
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Gate Capacitance

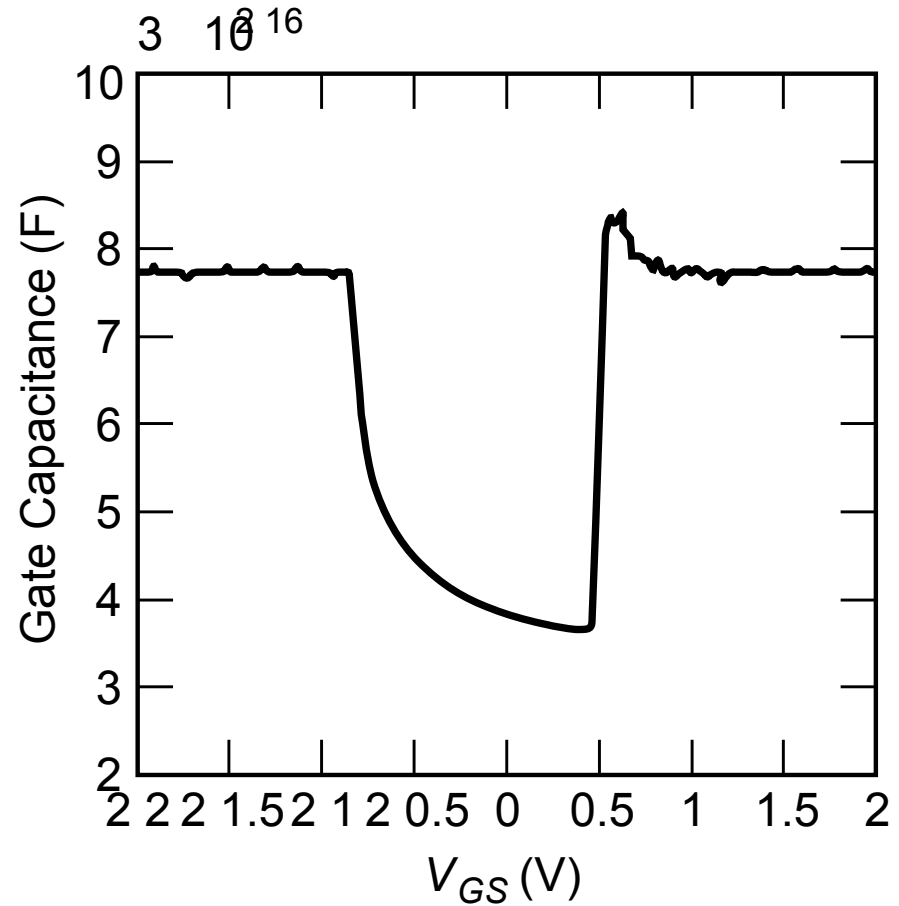
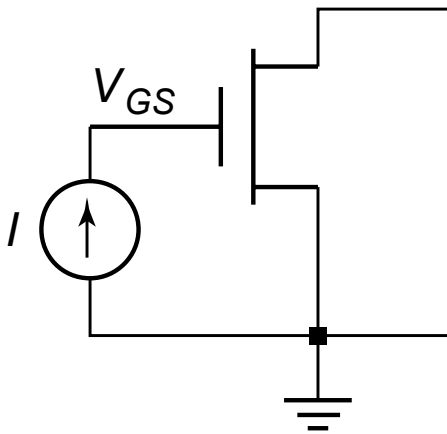


Capacitance as a function of V_{GS}
(with $V_{DS} = 0$)

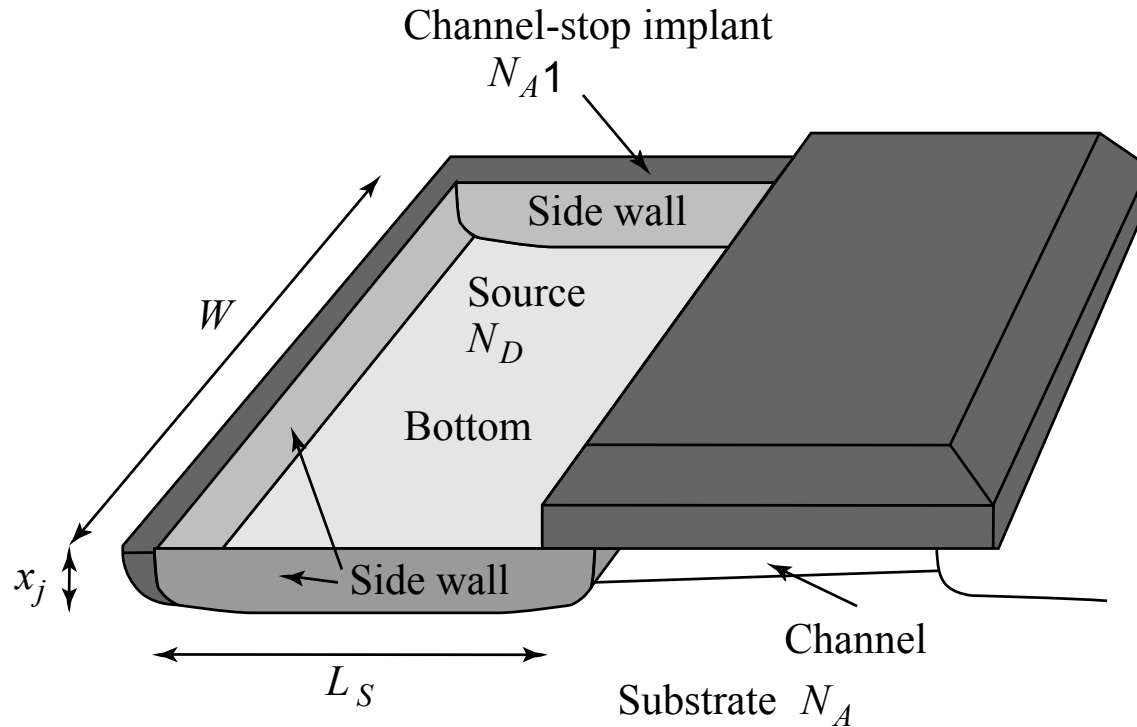


Capacitance as a function of the
degree of saturation

Measuring the Gate Cap



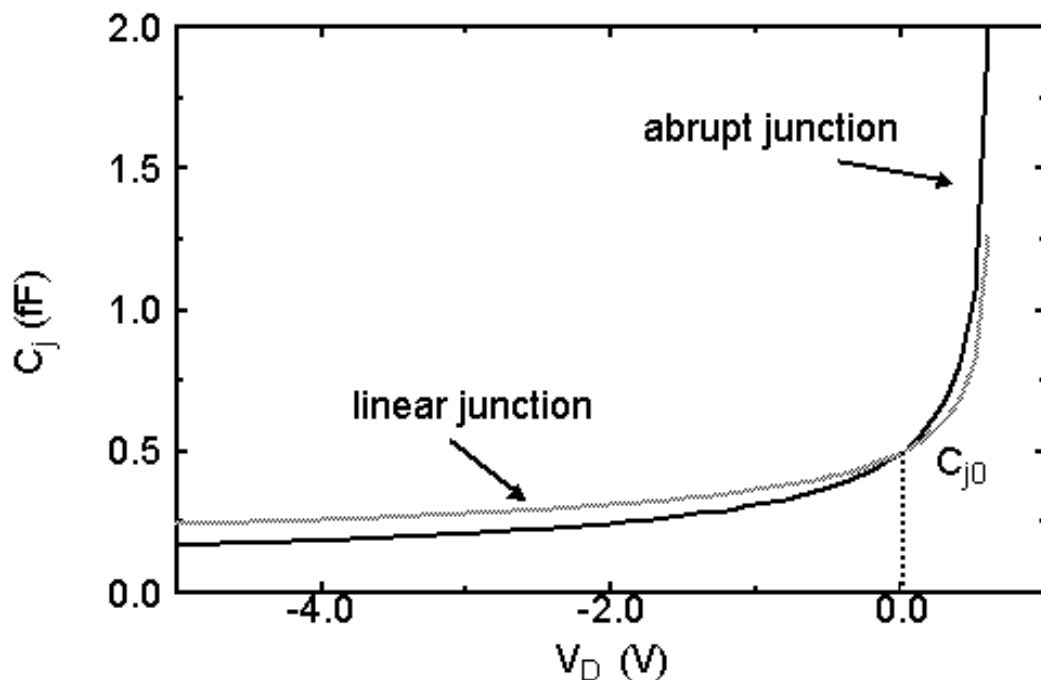
Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$

$$= C_j L_S W + C_{jsw} (2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

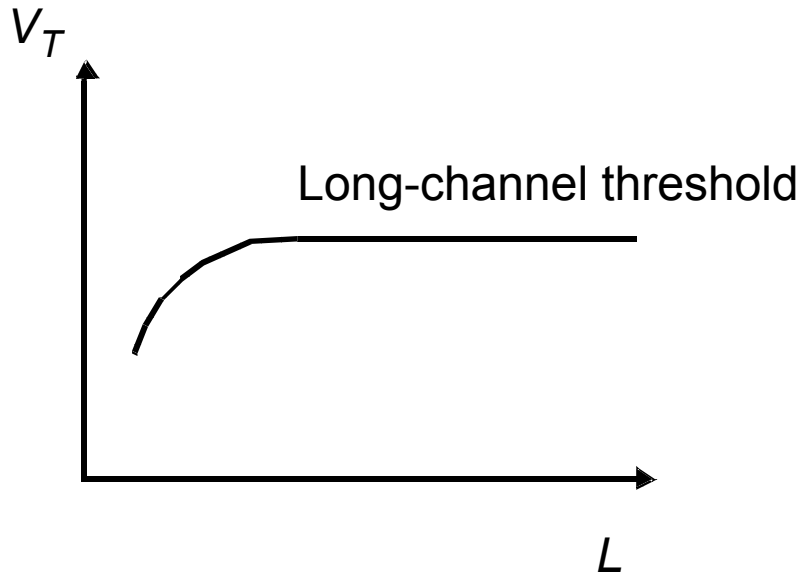
Capacitances in 0.25 μm CMOS process

	C_{ox} (fF/ μm^2)	C_{O} (fF/ μm)	C_j (fF/ μm^2)	m_j	ϕ_b (V)	$C_{j\text{sw}}$ (fF/ μm)	$m_{j\text{sw}}$	$\phi_{b\text{sw}}$ (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

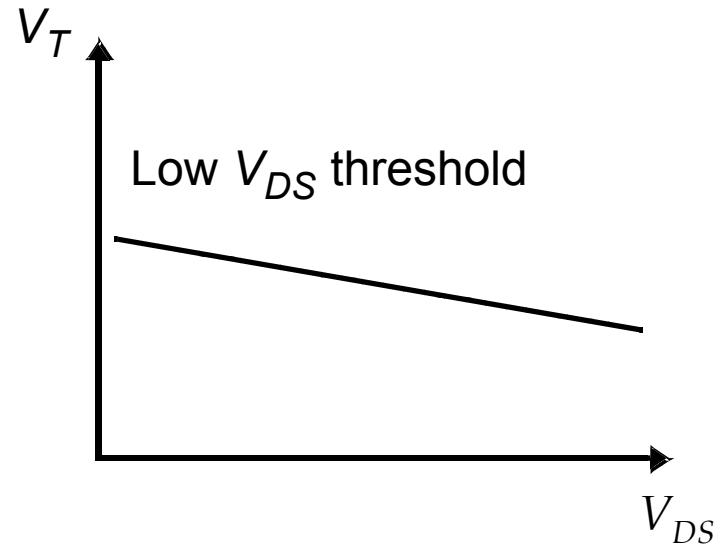
The Sub-Micron MOS Transistor

- ☐ **Threshold Variations**
- ☐ **Subthreshold Conduction**
- ☐ **Parasitic Resistances**

Threshold Variations

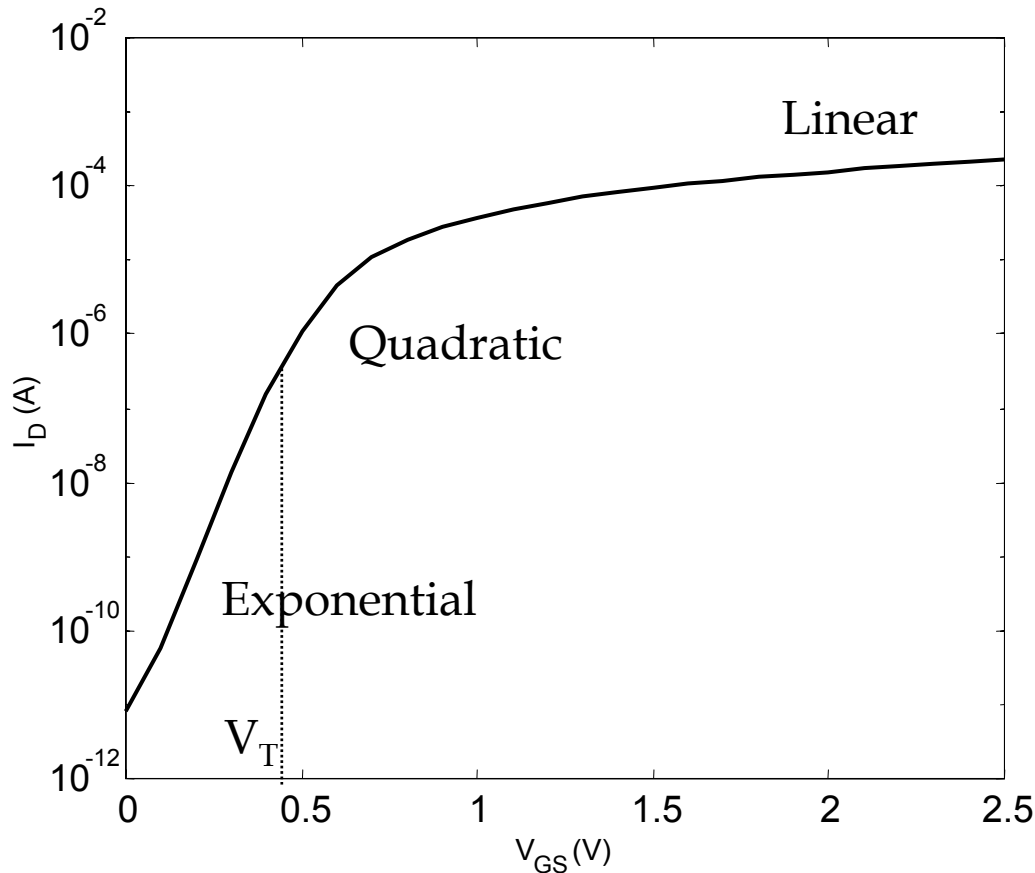


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Sub-Threshold Conduction



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

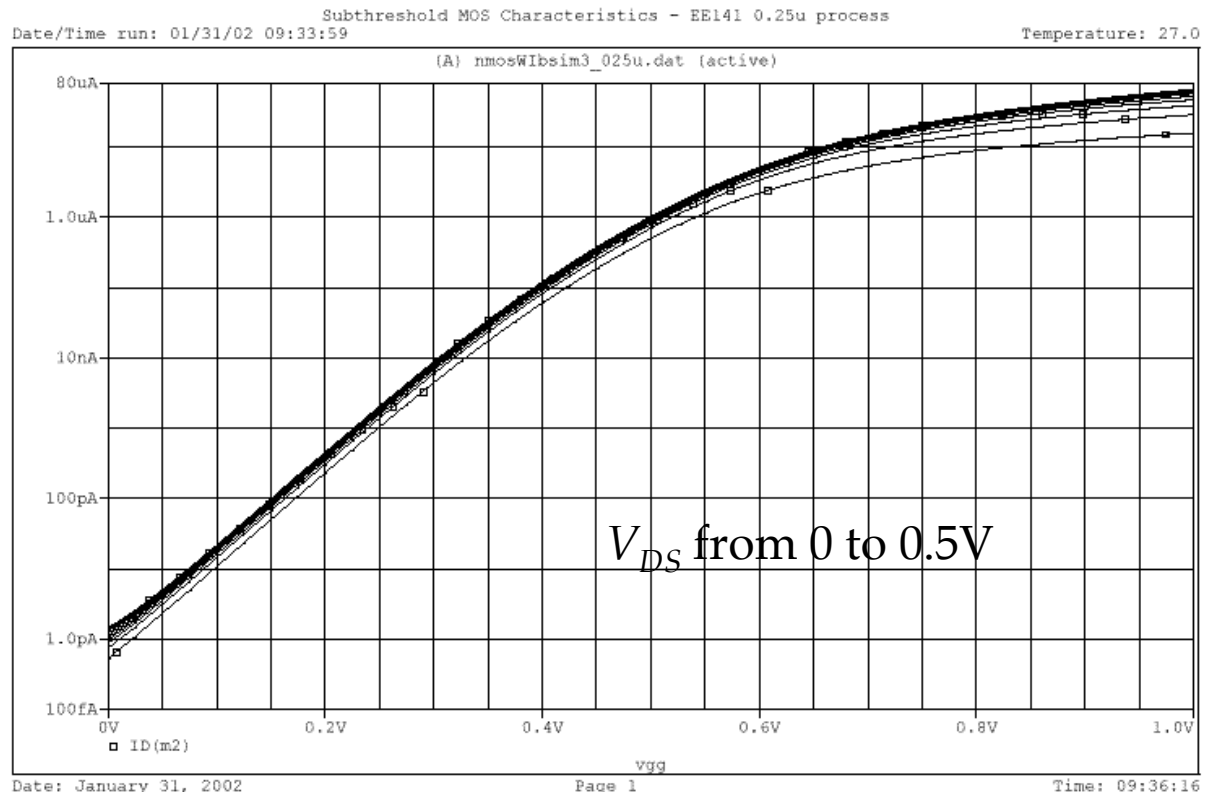
S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n \left(\frac{kT}{q} \right) \ln(10)$$

Typical values for S :
60 .. 100 mV/decade

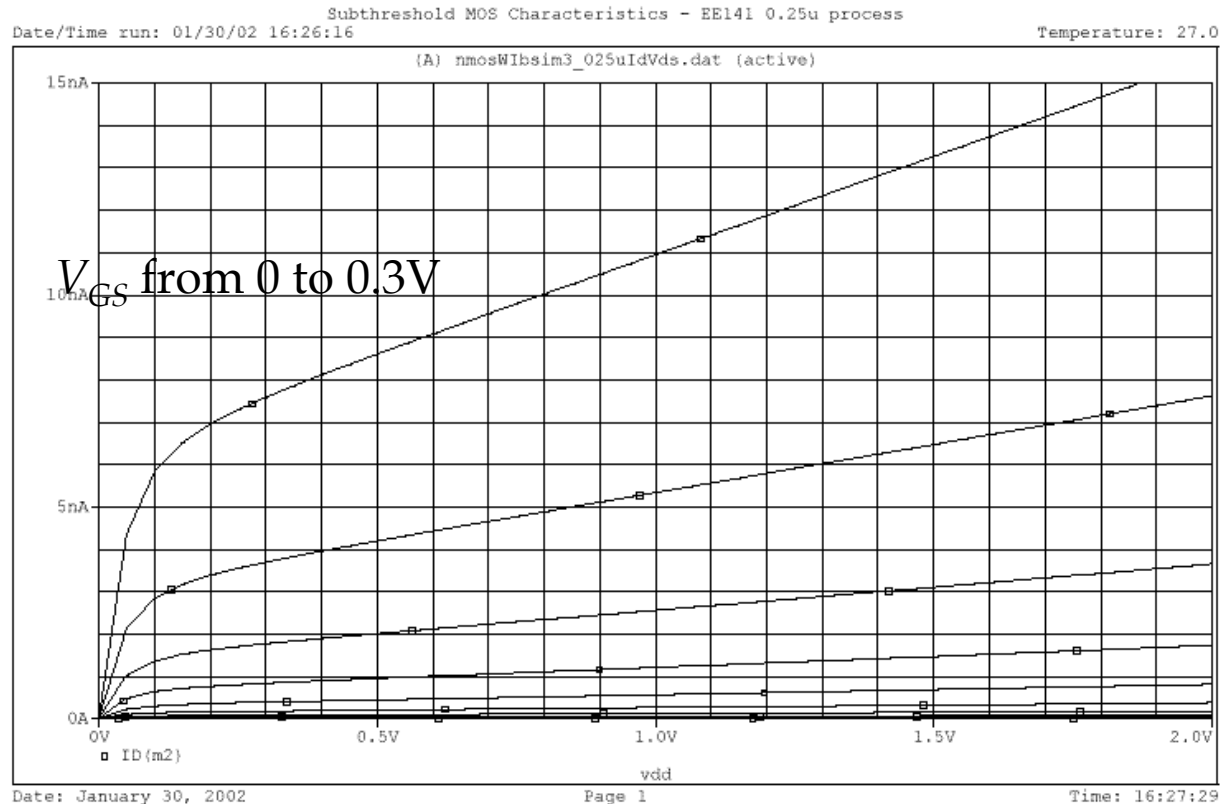
Sub-Threshold I_D vs V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right)$$



Sub-Threshold I_D vs V_{DS}

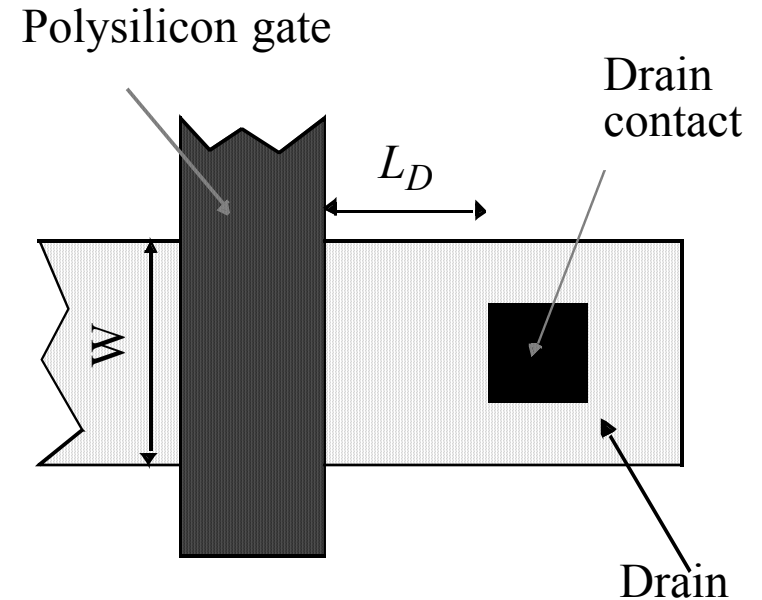
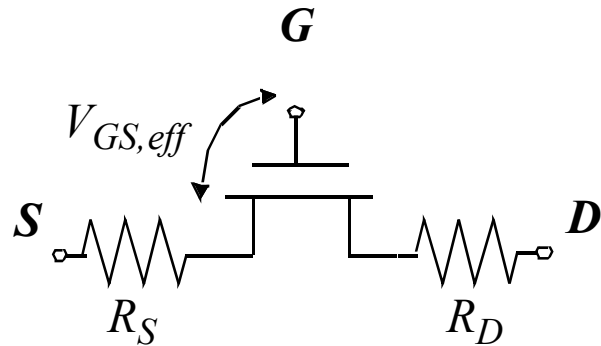
$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right) (1 + \lambda \cdot V_{DS})$$



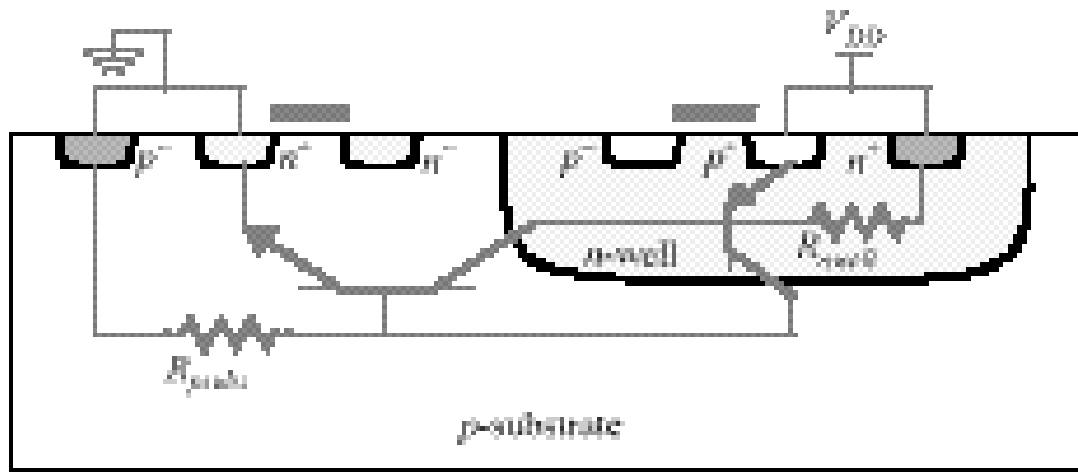
Summary of MOSFET Operating Regions

- Strong Inversion $V_{GS} > V_T$
 - Linear (Resistive) $V_{DS} < V_{DSAT}$
 - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
 - Exponential in V_{GS} with linear V_{DS} dependence

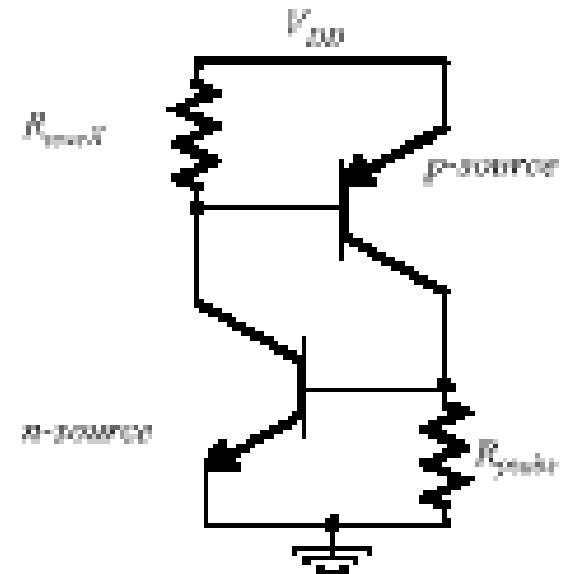
Parasitic Resistances



Latch-up

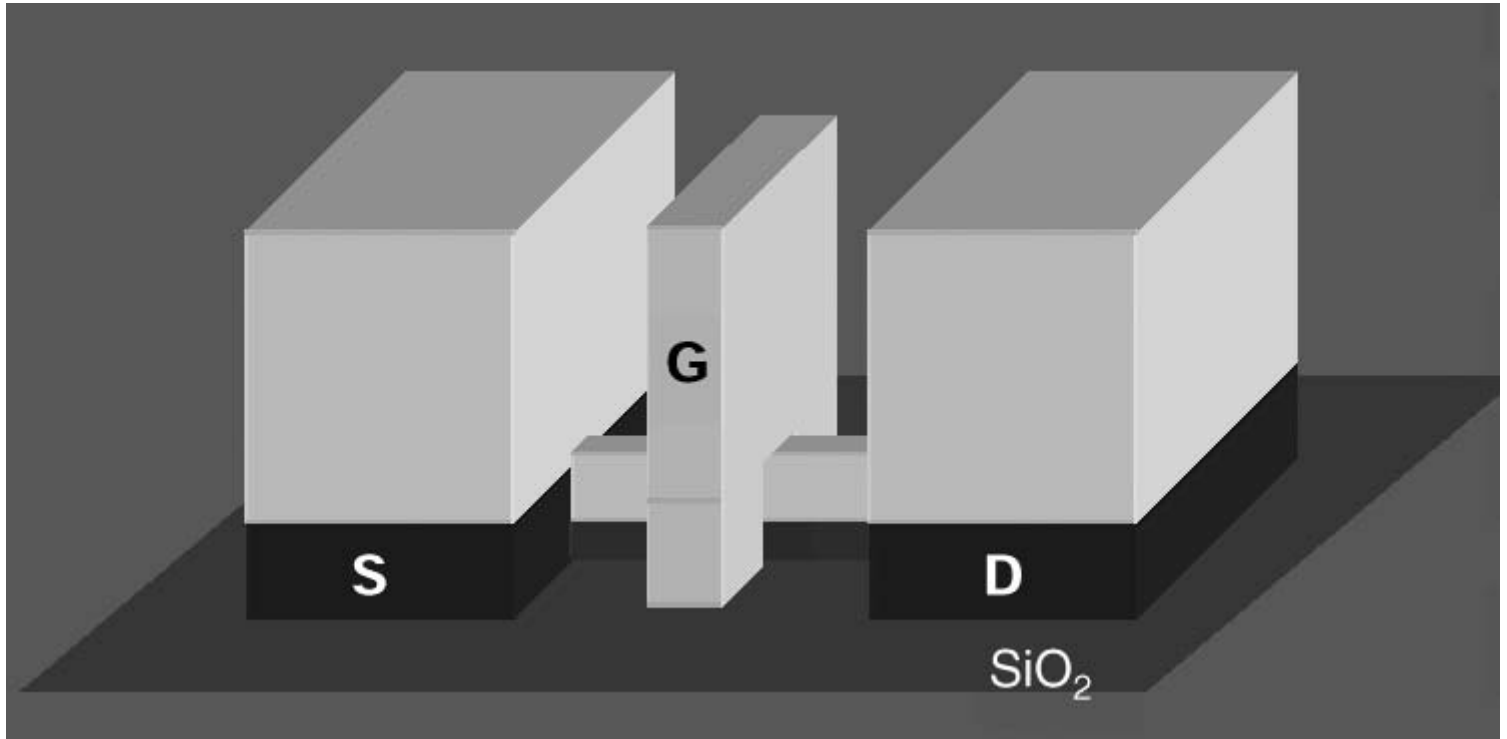


(a) Origin of latchup



(b) Equivalent circuit

Future Perspectives



25 nm FINFET MOS transistor