



Digital Integrated Circuits

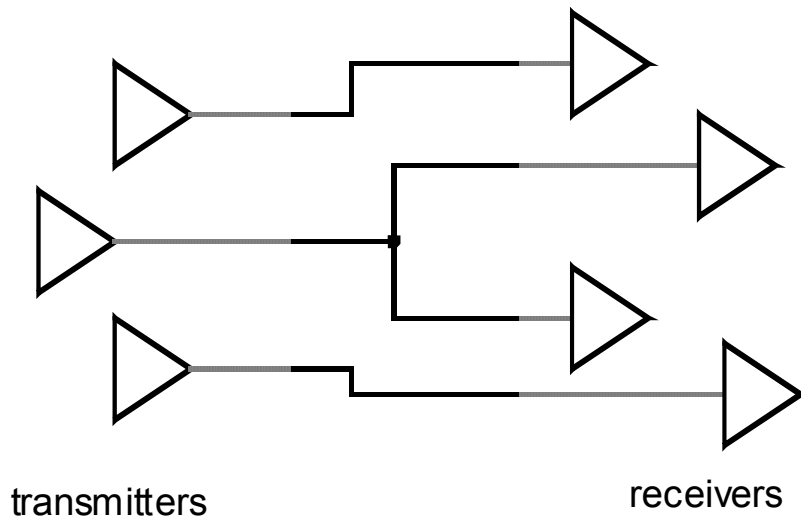
A Design Perspective

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Anantha Chandrakasan
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The Wire

July 30, 2002

The Wire

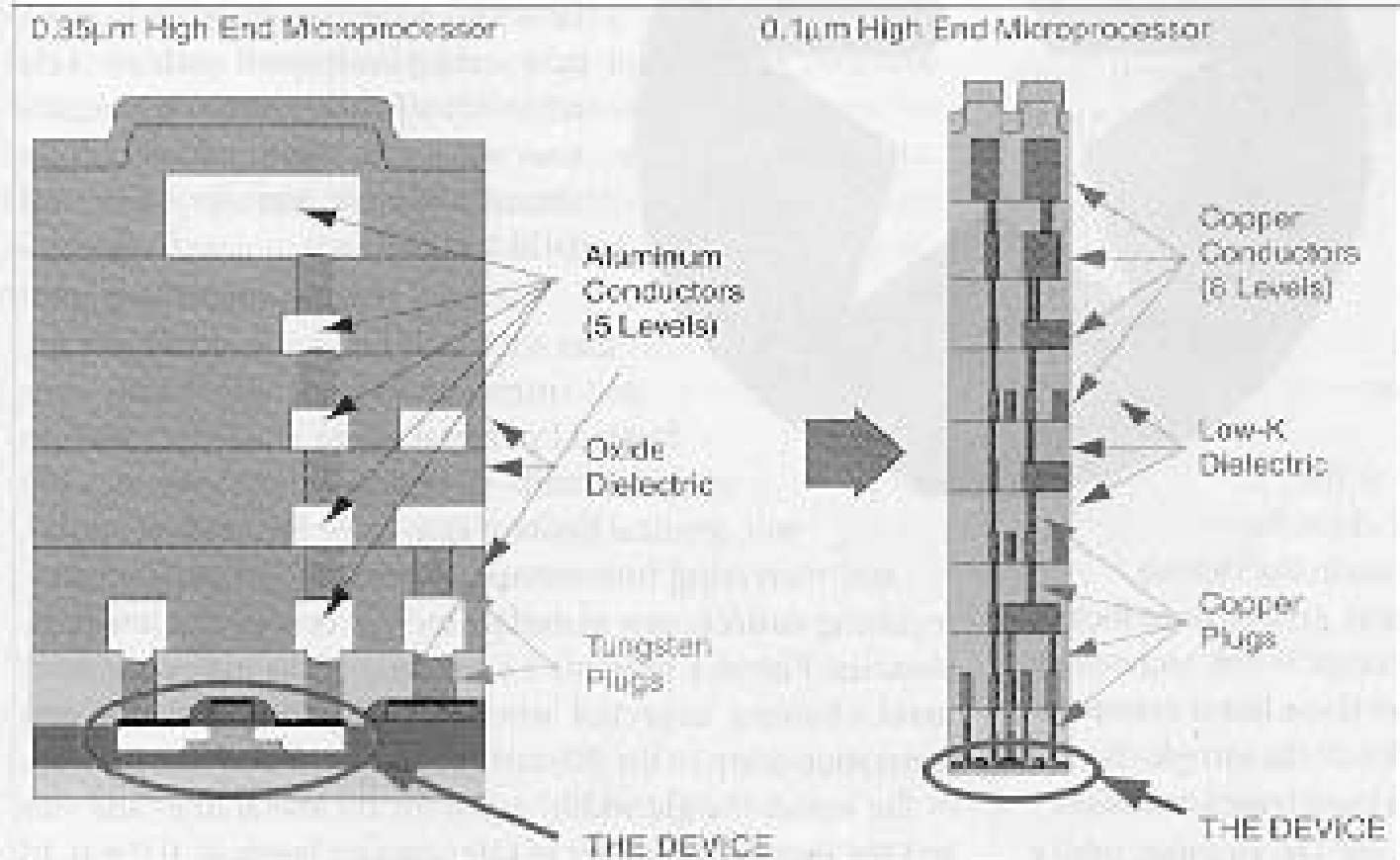


schematics



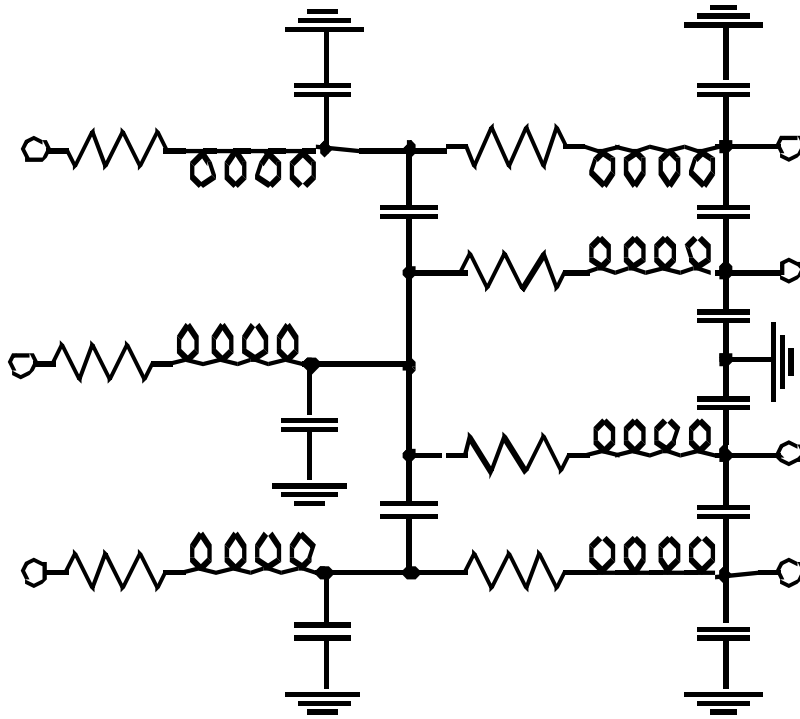
physical

Interconnect Impact on Chip

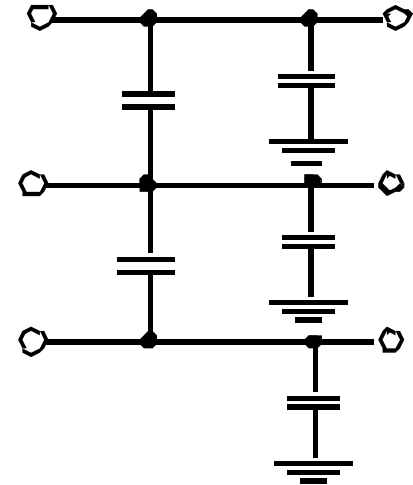


1. Process architecture challenge.

Wire Models



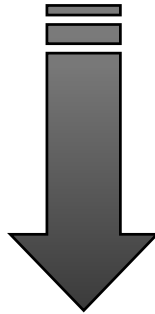
All-inclusive model



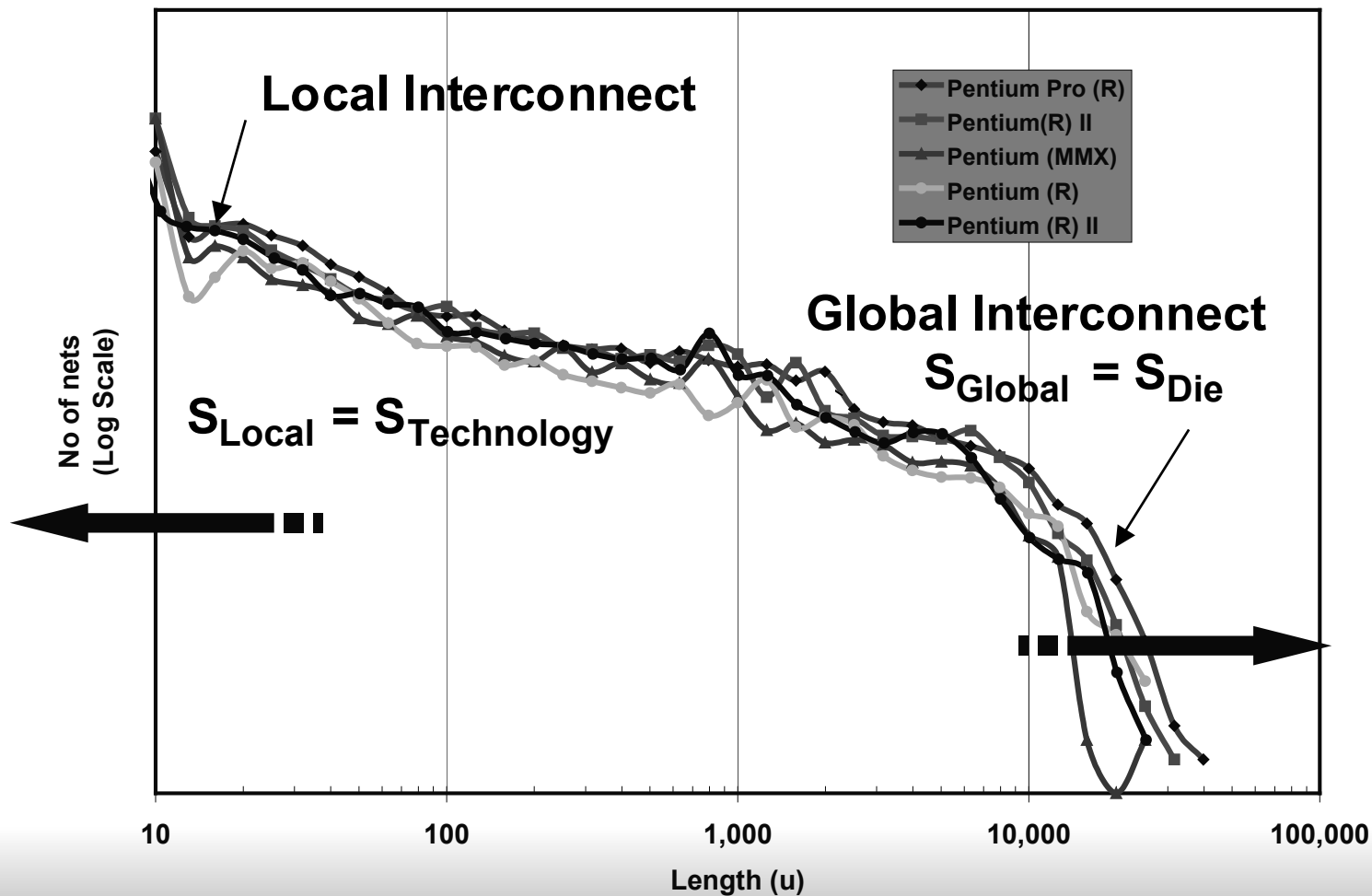
Capacitance-only

Impact of Interconnect Parasitics

- ❑ Interconnect parasitics
 - reduce reliability
 - affect performance and power consumption
- ❑ Classes of parasitics
 - Capacitive
 - Resistive
 - Inductive



Nature of Interconnect



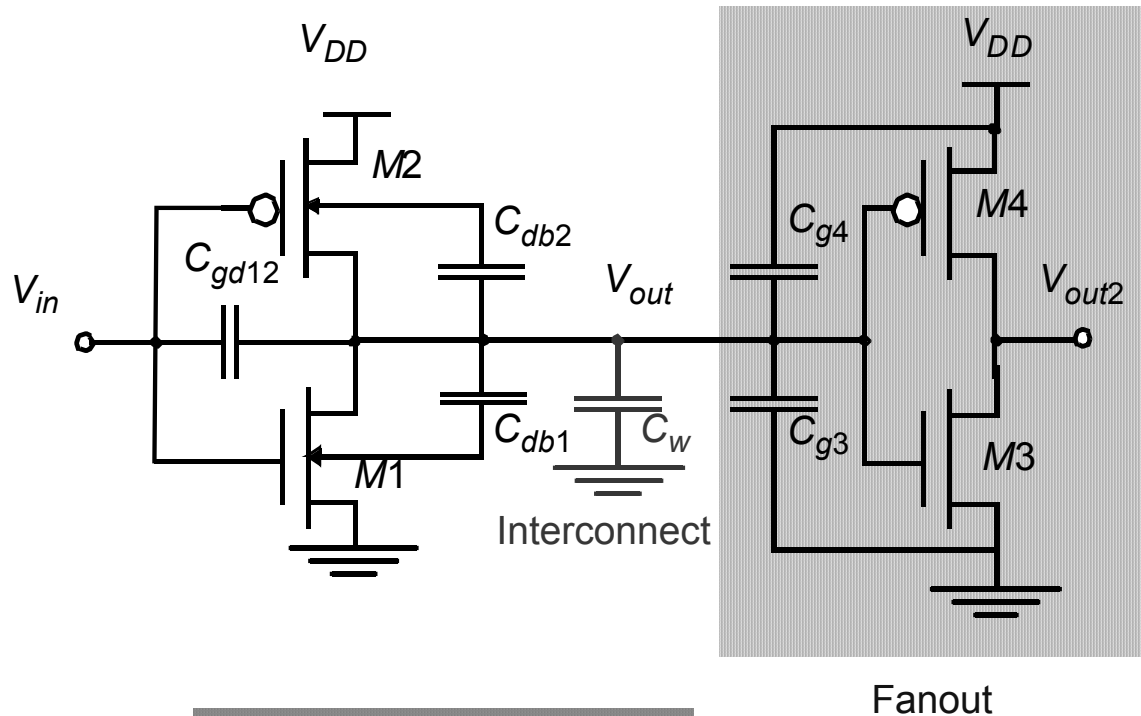
Source: Intel

INTERCONNECT

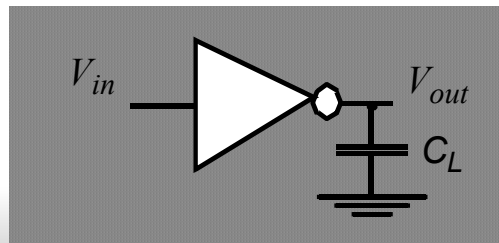
Capacitance



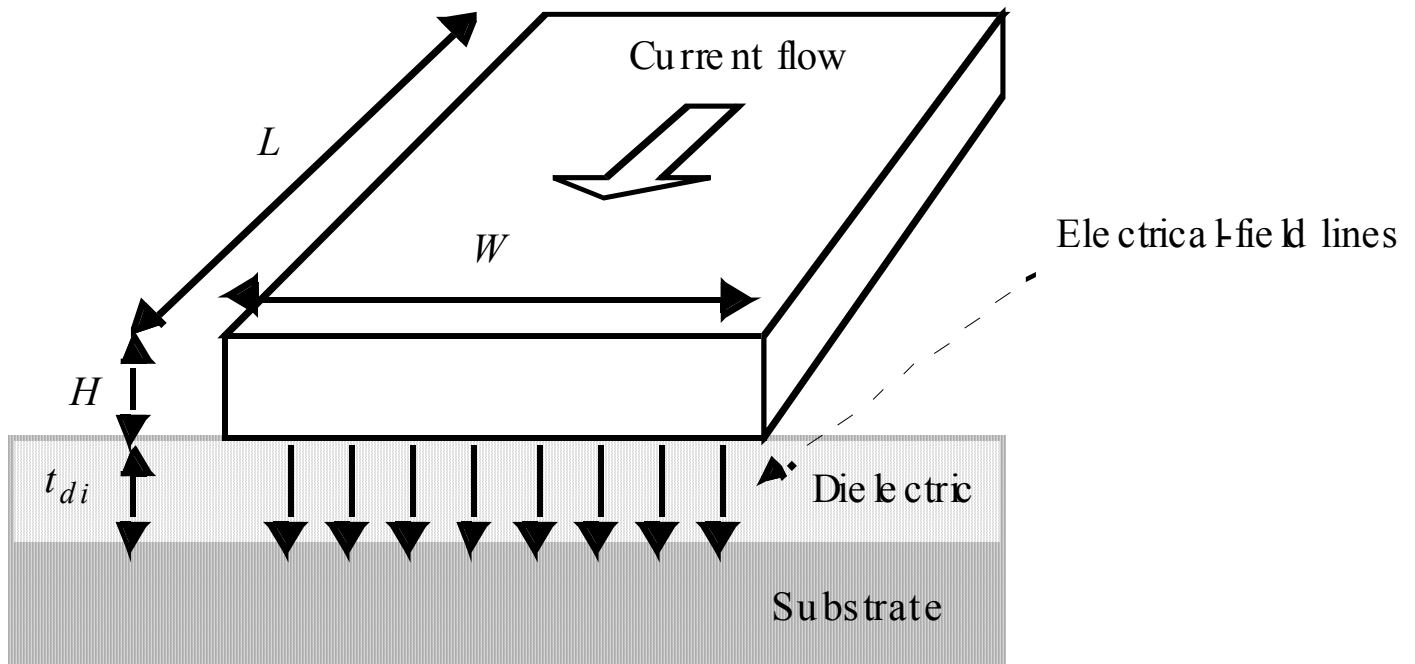
Capacitance of Wire Interconnect



Simplified Model



Capacitance: The Parallel Plate Model



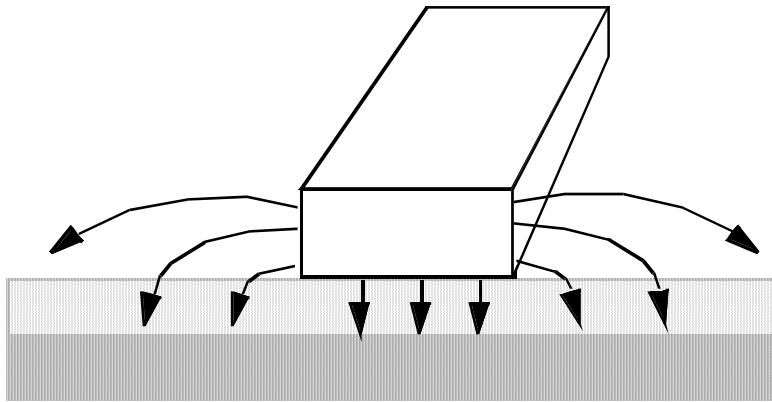
$$C_{int} = \frac{\epsilon_{di}}{t_{di}} WL$$

$$S_{Cwire} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

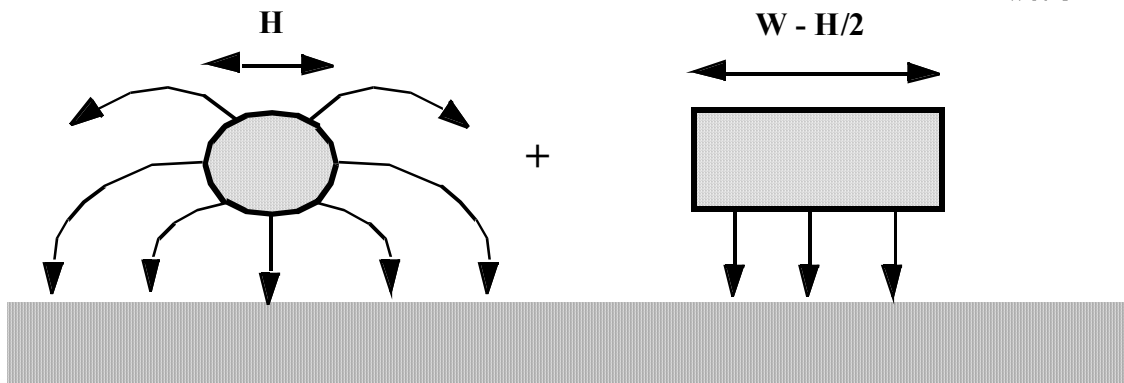
Permittivity

Material	ϵ_r
Free space	1
Aerogels	~ 1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance



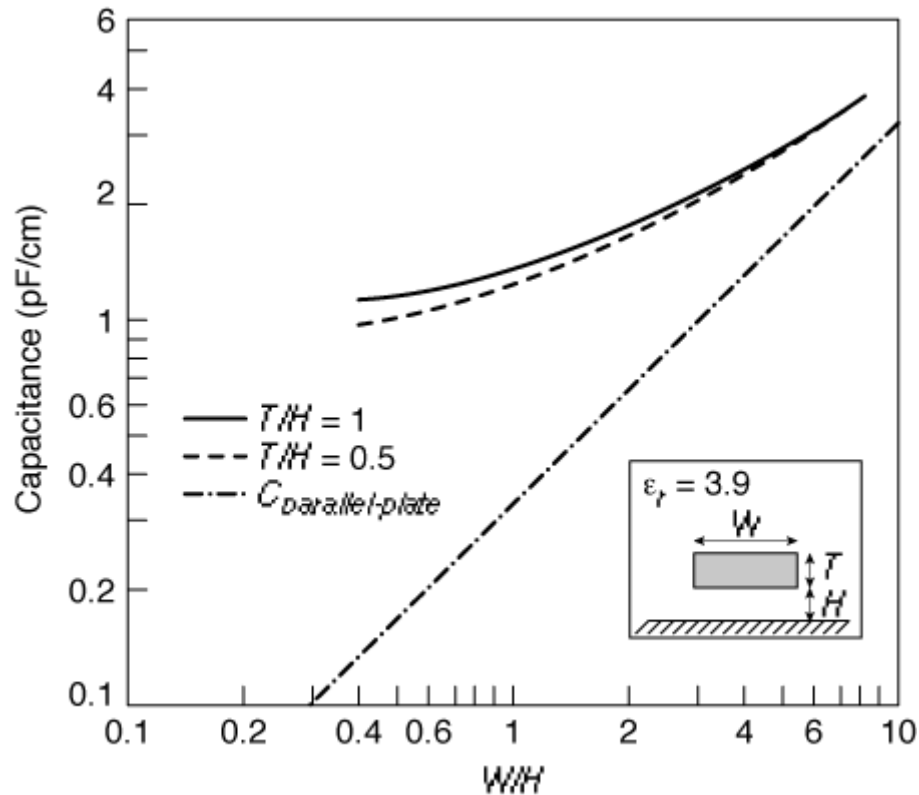
(a)



(b)

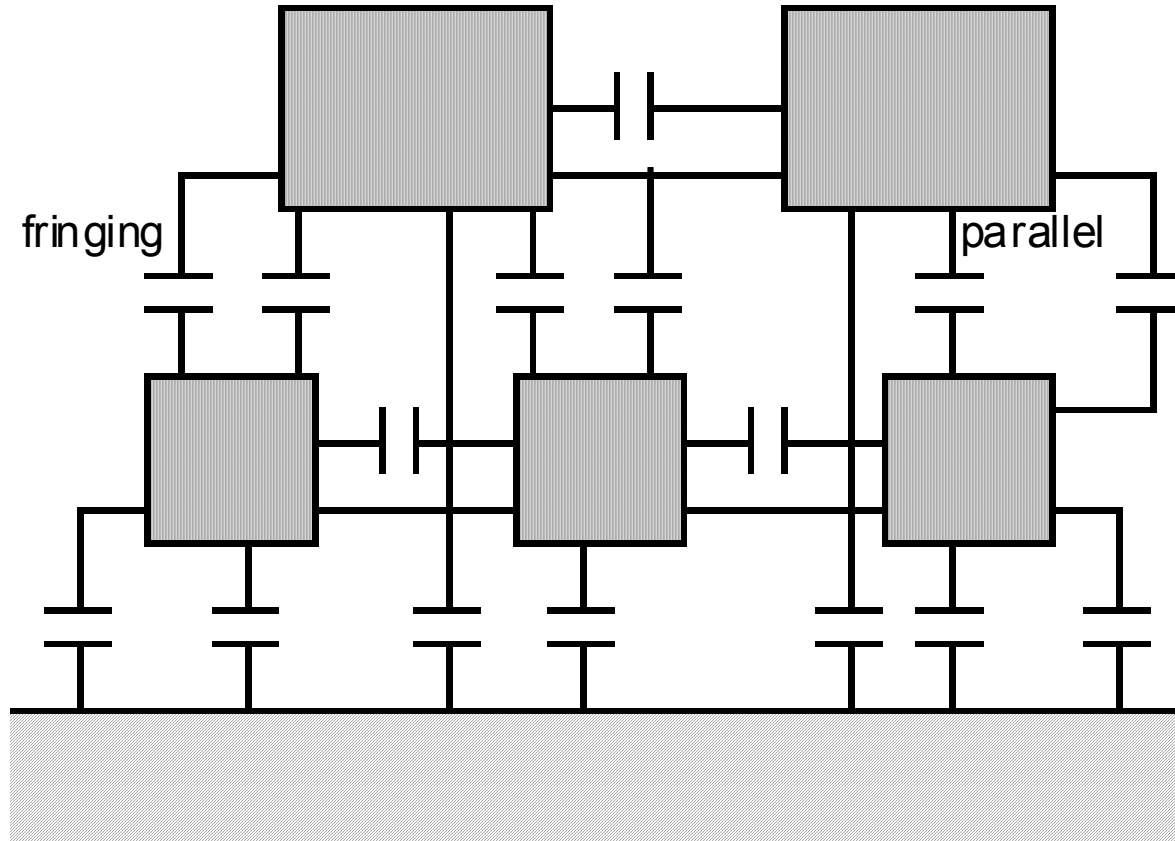
$$C_{wire} = C_{pp} + C_{fringe} = \frac{w\epsilon_{di}}{t_{di}} + \frac{2\pi\epsilon_{di}}{\log(t_{di}/H)}$$

Fringing versus Parallel Plate

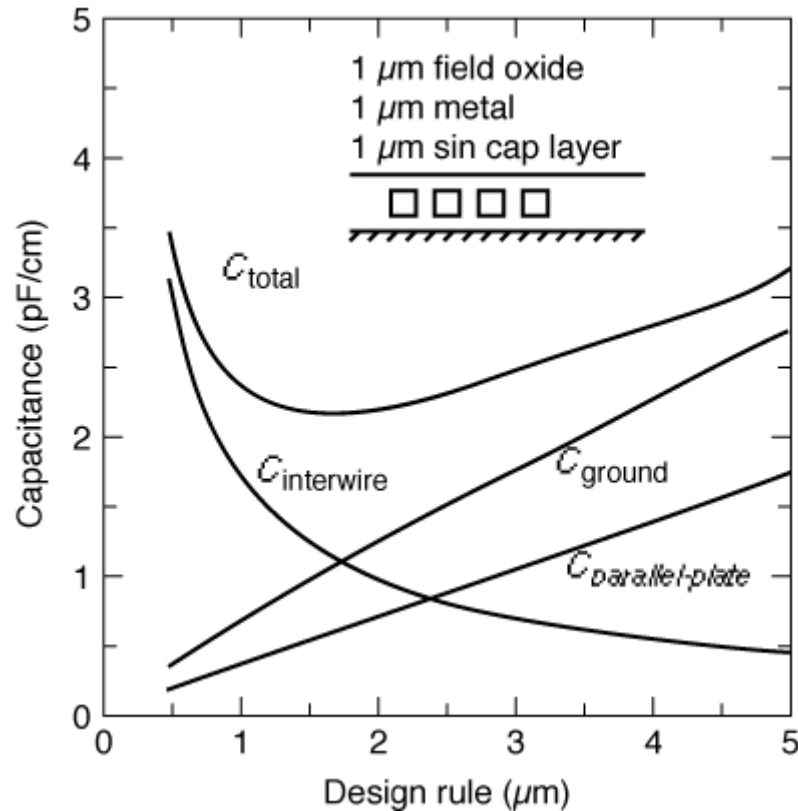


(from [Bakoglu89])

Interwire Capacitance



Impact of Interwire Capacitance



(from [Bakoglu89])

Wiring Capacitances (0.25 μm CMOS)

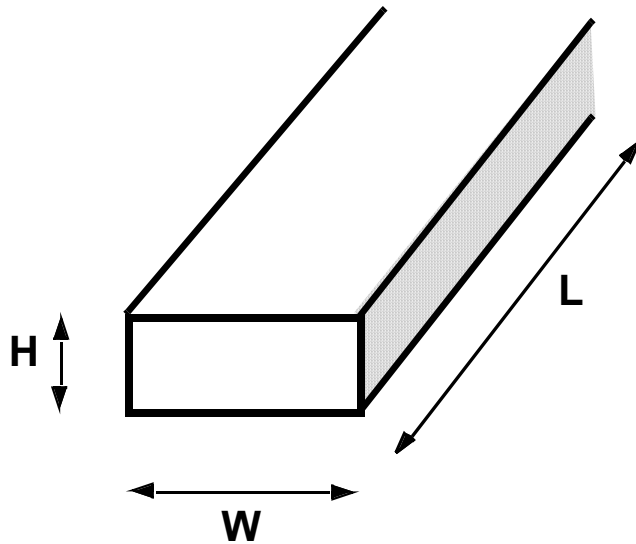
	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

INTERCONNECT

Resistance

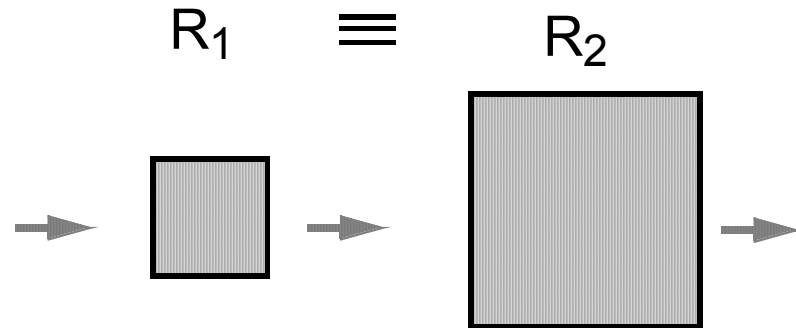


Wire Resistance



$$R = \frac{\rho L}{HW}$$

Sheet Resistance
 R_0



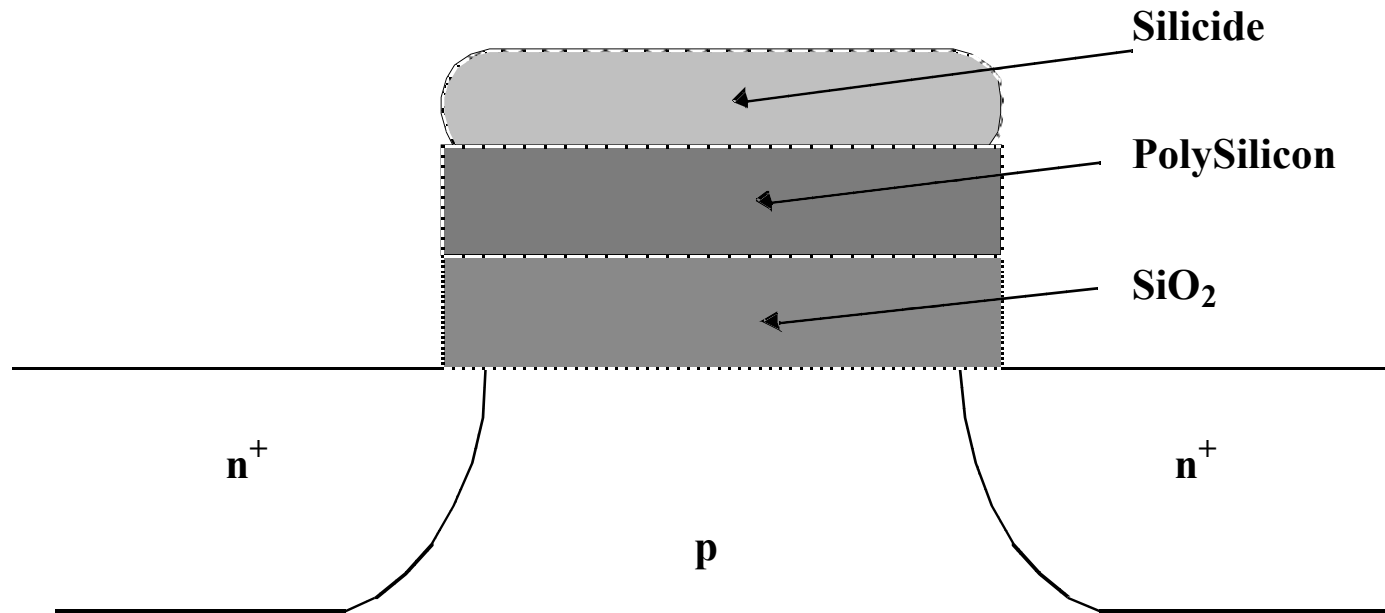
Interconnect Resistance

Material	ρ ($\Omega\text{-m}$)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- ❑ **Selective Technology Scaling**
- ❑ **Use Better Interconnect Materials**
 - reduce average wire-length
 - e.g. copper, silicides
- ❑ **More Interconnect Layers**
 - reduce average wire-length

Polycide Gate MOSFET



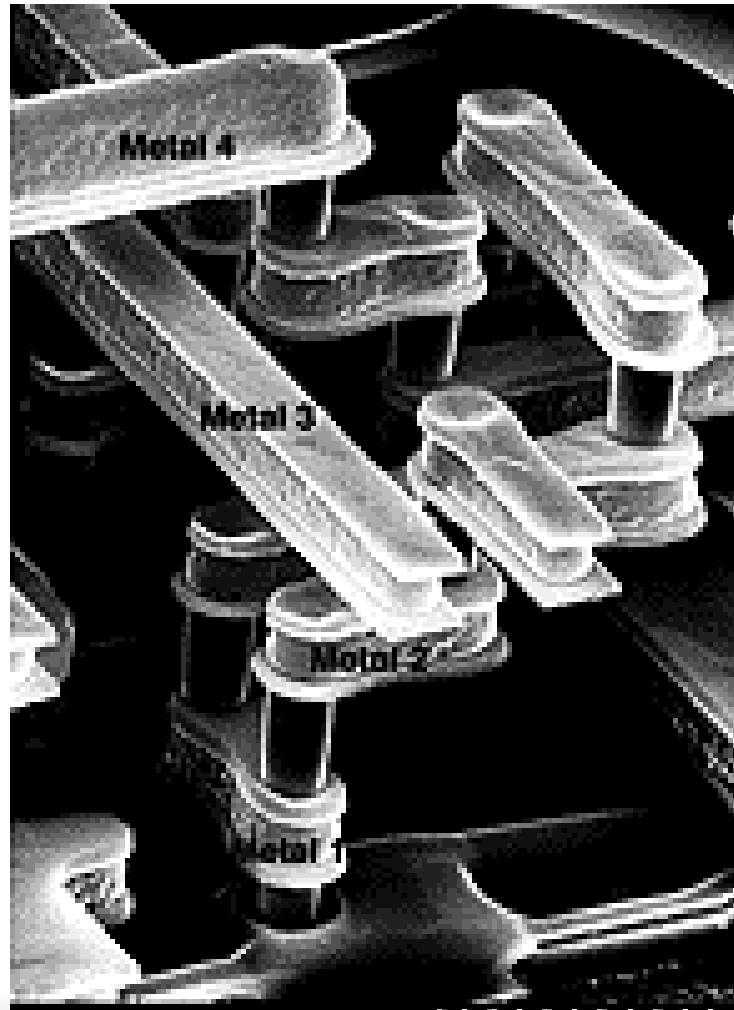
Silicides: WSi₂, TiSi₂, PtSi₂ and TaSi

Conductivity: 8-10 times better than Poly

Sheet Resistance

Material	Sheet Resistance (Ω/\square)
n- or p-well diffusion	1000 – 1500
n^+ , p^+ diffusion	50 – 150
n^+ , p^+ diffusion with silicide	3 – 5
n^+ , p^+ polysilicon	150 – 200
n^+ , p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Modern Interconnect



Example: Intel 0.25 micron Process

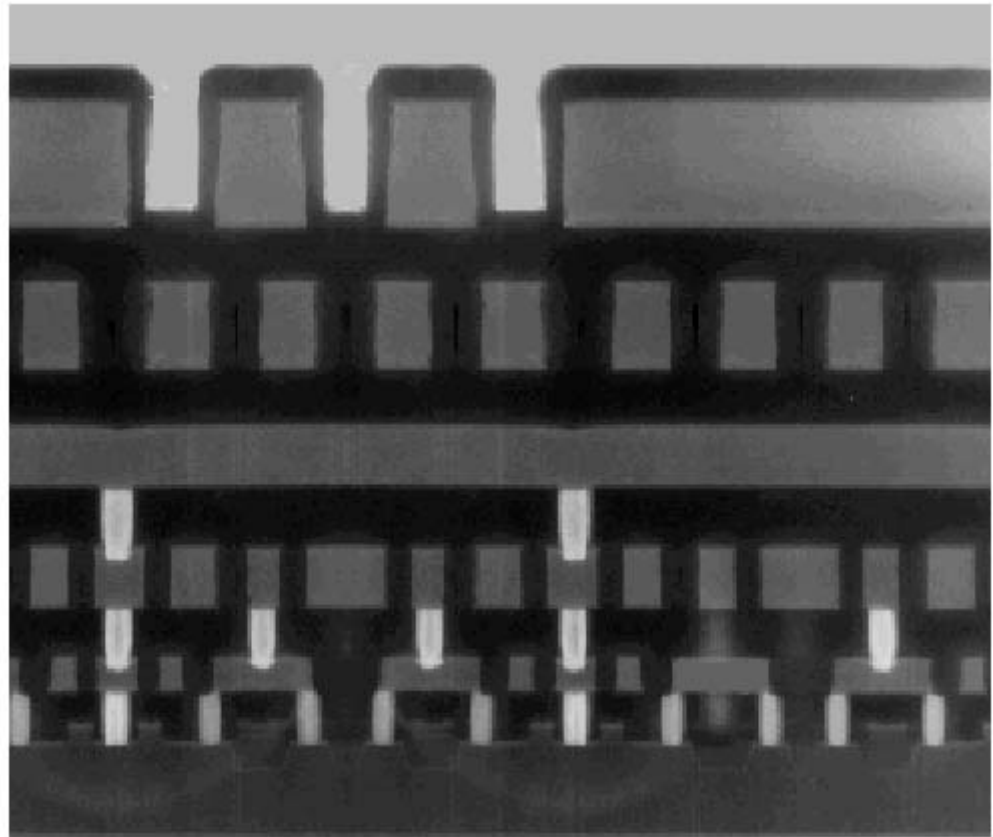
5 metal layers

Ti/Al - Cu/Ti/TiN

Polysilicon dielectric

<u>LAYER</u>	<u>PITCH</u>	<u>THICK</u>	<u>A.R.</u>
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	μm	μm	

Layer pitch, thickness and aspect ratio



INTERCONNECT

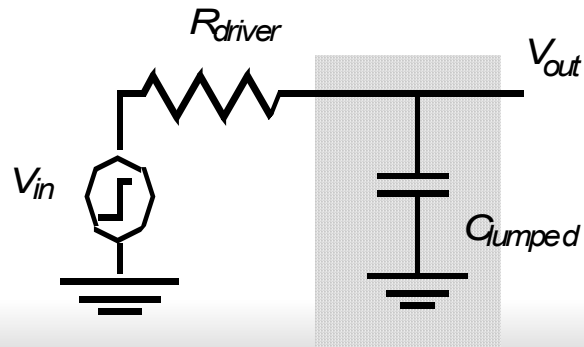
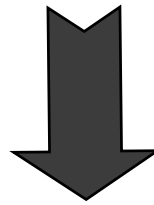
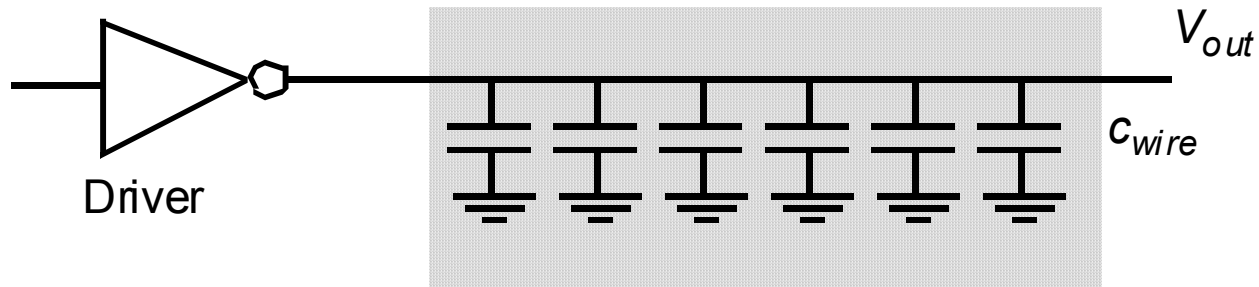
Inductance





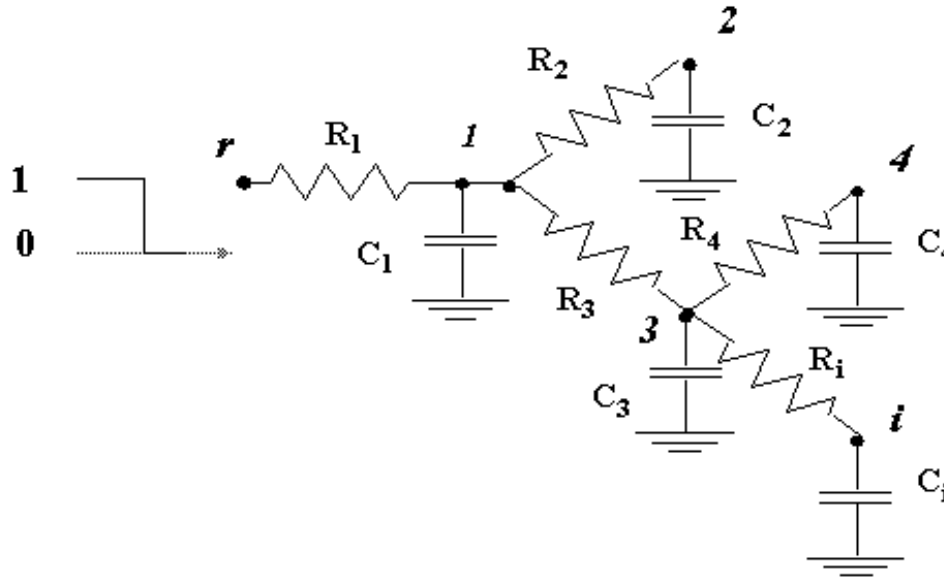
Interconnect Modeling

The Lumped Model



The Lumped RC-Model

The Elmore Delay

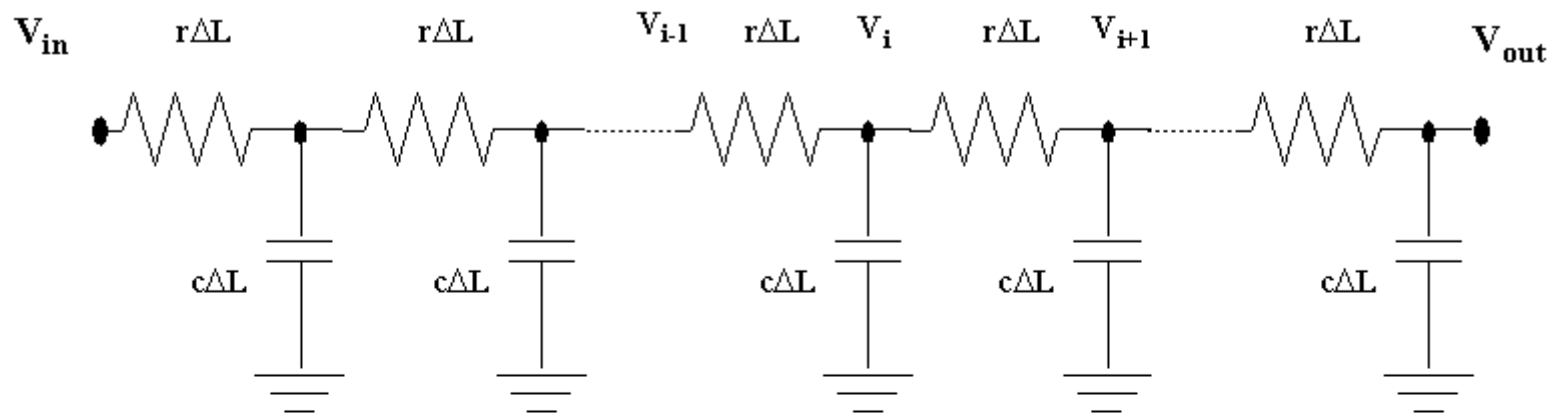


$$R_{ik} = \sum_{j=1}^N R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

The Ellmore Delay

RC Chain



$$\tau_N = \sum_{i=1}^N R_i \sum_{j=i}^N C_j = \sum_{i=1}^N C_i \sum_{j=1}^i R_j$$

Wire Model

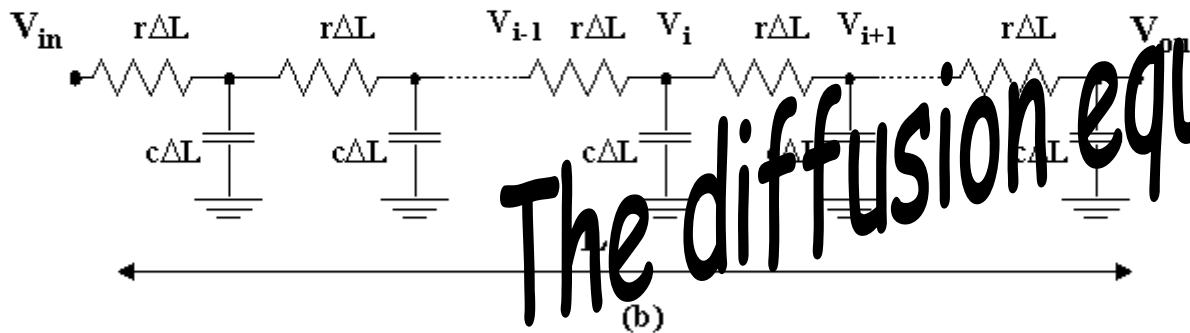
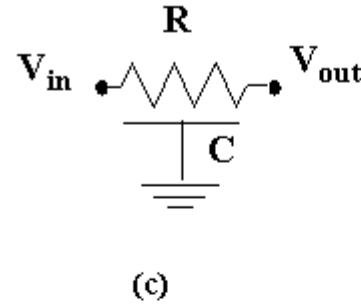
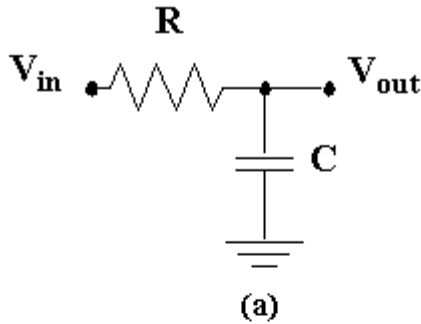
Assume: Wire modeled by N equal-length segments

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \dots + Nrc) = (rcL^2) \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N}$$

For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

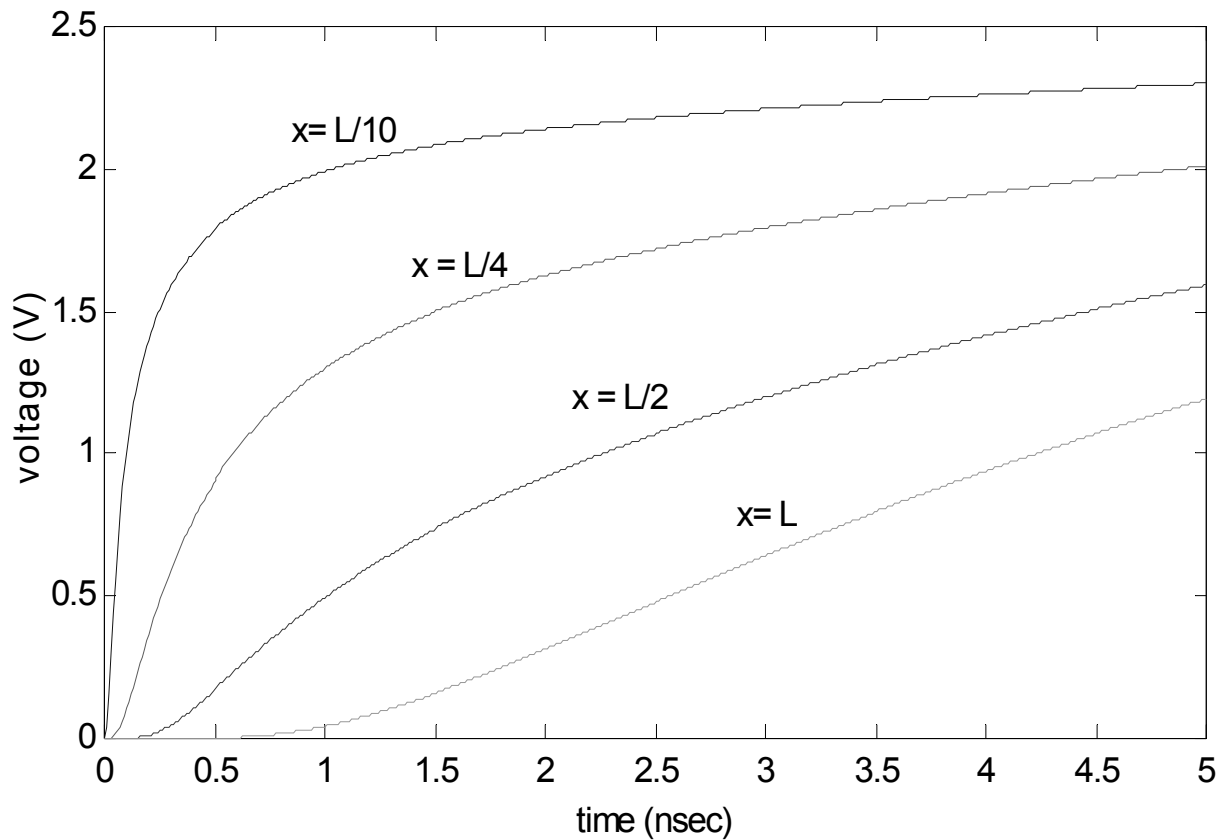
The Distributed RC-line



The diffusion equation

$$\tau(V_{out}) = \frac{rc L^2}{2}$$

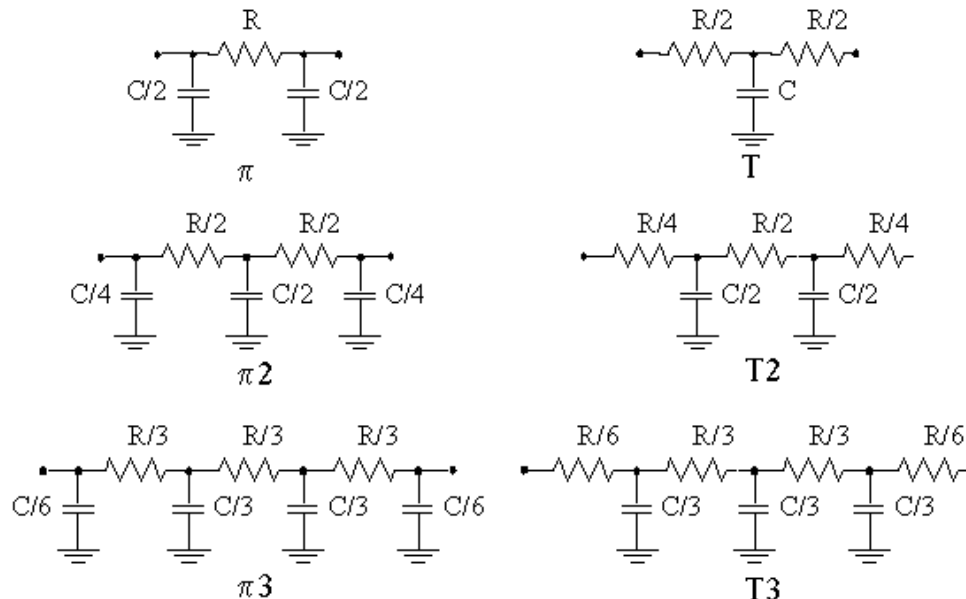
Step-response of RC wire as a function of time and space



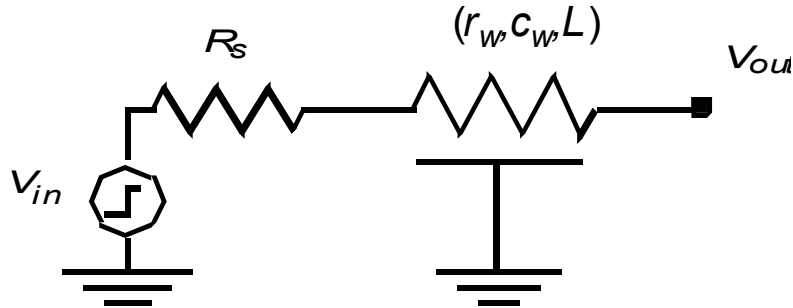
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_T)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks:
Points of Interest.



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

Design Rules of Thumb

- rc delays should only be considered when $t_{pRC} \gg t_{pgate}$ of the driving gate

$$L_{crit} \gg \sqrt{t_{pgate}/0.38rc}$$

- rc delays should only be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

- when not met, the change in the signal is slower than the propagation delay of the wire